December 19, 2005 - Final Exam

Name: _____

Recitation: _____

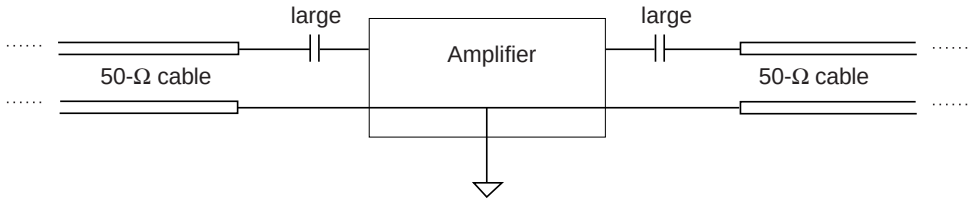
problem	grade
1	
2	
3	
4	
total	

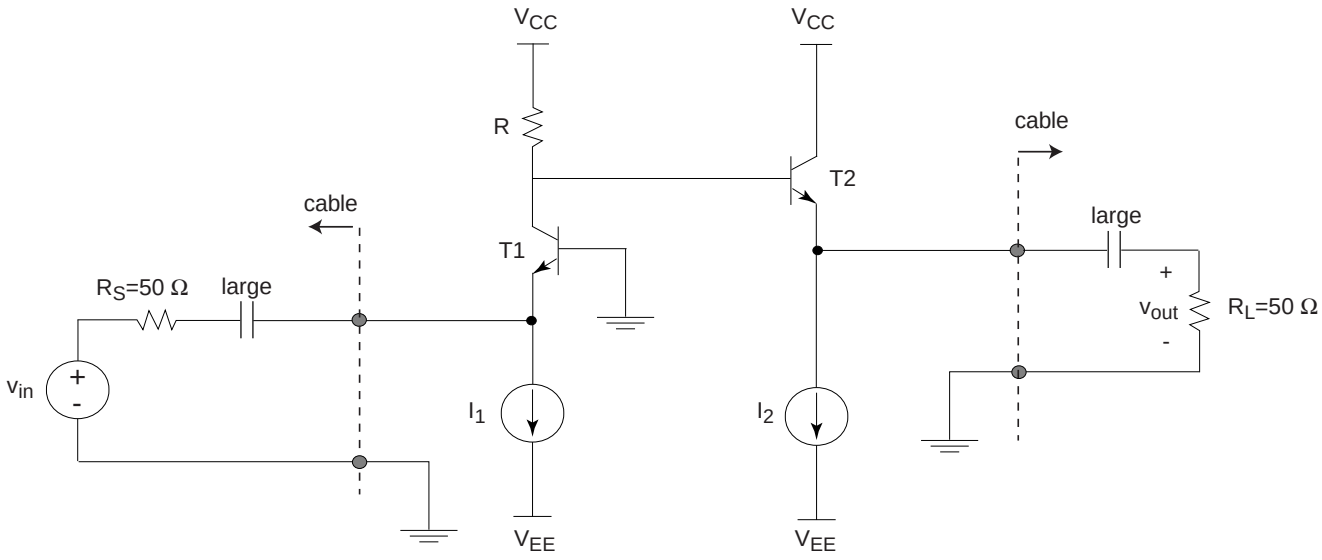
General guidelines (please read carefully before starting):

- Make sure to write your name on the space designated above.
- **Open book**: you can use any material you wish.
- All answers should be given in the space provided. Please do not turn in any extra material. If you need more space, use the back of the page.
- You have **three hours** to complete your exam.
- Make reasonable approximations and *state them*, i.e. quasi-neutrality, depletion approximation, etc.
- Partial credit will be given for setting up problems without calculations. **NO** credit will be given for answers without reasons.
- Use the symbols utilized in class for the various physical parameters, i.e. μ_n, I_D, E, etc.
- Every numerical answer must have the proper units next to it. Points will be subtracted for answers without units or with wrong units.
- Use $\phi = 0$ at $n_o = p_o = n_i$ as potential reference.
- Use the following fundamental constants and physical parameters for silicon and silicon dioxide at room temperature:

$n_i = 1 \times 10^{10}\ cm^{-3}$
$kT/q = 0.025\ V$
$q = 1.60 \times 10^{-19}\ C$
$\epsilon_s = 1.05 \times 10^{-12}\ F/cm$
$\epsilon_{ox} = 3.45 \times 10^{-13}\ F/cm$

1. *(28 points)* This problem studies an amplifier designed to boost a high-frequency signal midway along a 50-Ω cable. A block diagram of the cable and amplifier is shown below, together with the corresponding circuit.





In studying the amplifier, make use of the following information:

- To avoid undesired reflections within the input and output cables, the amplifier must be designed to have a 50 Ω input resistance and a 50 Ω output resistance. (To learn why, take 6.013!)
- The coupling capacitors in the block diagram and circuit isolate the biasing inside the amplifier from the cables. Assume the capacitors are large enough to be short circuits for the purposes of all small-signal modeling.
- Assume that both transistors in the amplifier exhibit the same forward current gain β, the same base-emitter capacitance C_π, and the same base-collector capacitance C_μ. When numerical values are needed, let $\beta_F = 200$, $C_\pi = 1$ pF, and $C_\mu = 0.1$ pF. Also, let the thermal voltage V_{th} be 25 mV. For both transistors, ignore their small-signal collector-emitter output resistance until Part 1i).
- Assume that the two bias current sources in the amplifier, I_1 and I_2, are ideal (*i.e.* their associated internal resistance is infinity).

1a) *(4 points)* The amplifier comprises two stages. For each of the following objectives, explain in a few sentences why the amplifier might be well-suited to meeting the objective.

□ 50-Ω Input Resistance:

□ 50-Ω Output Resistance:

□ High Voltage Gain:

□ High Bandwidth:

1b) *(10 points)* Draw a small-signal circuit model of the entire amplifier including the Thevenin equivalent of the input cable, and the equivalent resistive load of the output cable. (Again, ignore the coupling capacitors.) Clearly label the value of each component in the amplifier model in terms of R, I_1, I_2, β_F and V_{th}. If you choose to label the components with symbols such as g_{m} and R_π, make sure to express those symbols in terms R, I_1, I_2, β and V_{th}. *(Neat drawing and appropriate expressions expected).*

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1c) *(2 points) Analytically* determine the input resistance of the amplifier. Express the result in terms of R, I_1, I_2, β_F, V_{th}, and R_{L}.

1d) *(2 points)* What must be the *numerical* value of I_1 so that the input resistance found in Part (1c) is 50 Ω?

1e) *(2 points) Analytically* determine the output resistance of the amplifier. Express the result in terms of R, I_1, I_2, β_F, V_{th}, and R_{S}.

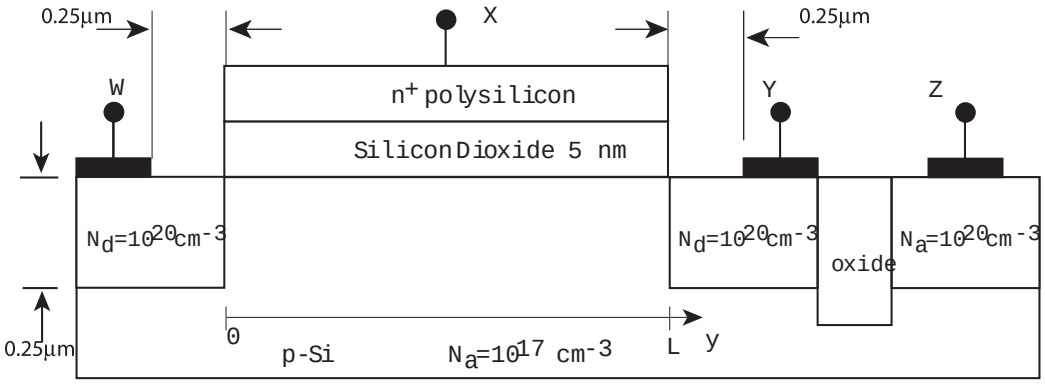
1f) *(2 points)* Assume that the amplifier has been designed to have a 50 Ω input resistance and a 50 Ω output resistance. In this case, *analytically* determine the small-signal midband gain of the amplifier from v_{in} to v_{out}. Express the results in terms of R, I_1, I_2, β, V_{th} and $R_{\text{S}} = R_{\text{L}} = 50\ \Omega$. To determine the small-signal midband gain, assume that C_π and C_μ are open circuits.

1g) *(2 points)* What must be the values of R and I_2 so that the output resistance is 50 Ω and the voltage gain is 25? *(Numerical values expected.)*

1h) *(2 points) Numerically* estimate the bandwidth of the amplifier under the assumption that it has been designed to provide a 50 Ω input resistance, a 50 Ω output resistance, and a midband gain of 25.

1i) *(2 points)* Assume that the Early Voltage of both transistors is 100 V. In a few sentences, explain why it is reasonable to ignore their collector-emitter output resistances during the analyses above.

2. *(21 points)* The device structure shown below has four terminals (W, X, Y, Z) and could be viewed as a n-channel MOSFET or a lateral npn bipolar transistor depending on the voltage applied to the various terminals. When operated as a MOSFET, $C_{ox} = 6.9 \times 10^{-7}\ F/cm^2$, $\gamma = 0.26\ V^{1/2}$, and $V_T = 0.11\ V$.



(2a) *(4 points)* If the device is to be operated as an n-channel MOSFET, identify the terminals *(answer W, X, Y, or Z in the space provided below)*:

Source: _____ Drain: _____ Gate: _____ Body: _____

(2b) *(3 points)* If the device is to be operated as a lateral npn BJT, identify the terminals *(answer W, X, Y, or Z in the space provided below).*

Emitter: _____ Base: _____ Collector: _____

(2c) *(2 points)* For the device shown above, what is the flatband voltage of the MOS capacitor formed by connecting terminals W, Y and Z to ground and varying the voltage in terminal X? *(Numerical answer expected).*

(2d) *(2 points)* We operate the device as a bipolar transistor with V_{XW} biased at the flatband voltage of the MOS capacitor. What is the collector current if the device is biased with $V_{CE} = 2\ V$ and $V_{BE} = 0.6\ V$? *(Numerical answer expected).*

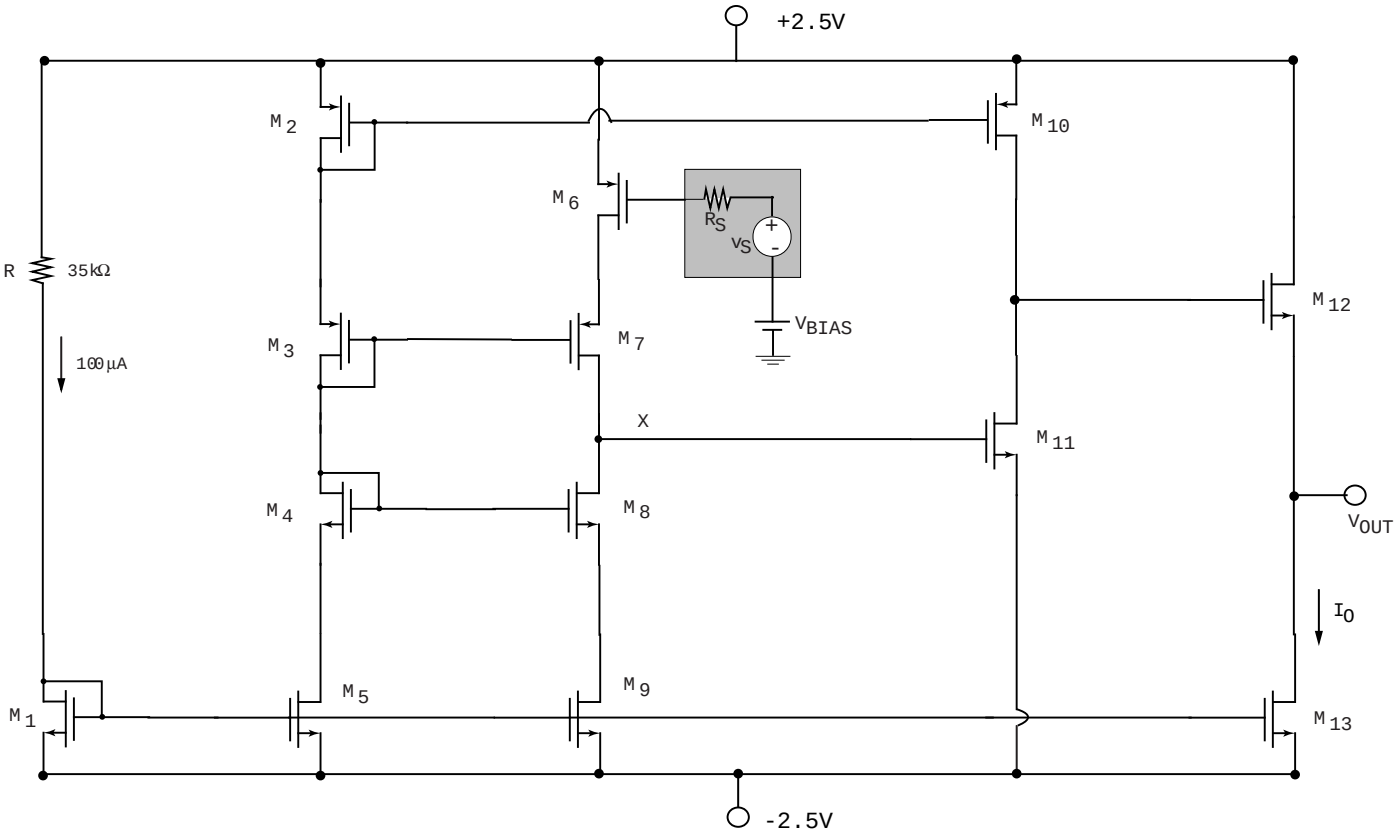
(2e) *(2 points)* What is the transit time of electrons across the base region of the BJT when the device is biased as in (2d)? *(Numerical answer expected).*

(2f) *(4 points)* Now we operate the device as a bipolar transistor with $V_{XW} = 0\ V$. What is the collector current if the device is biased with $V_{CE} = 2\ V$ and $V_{BE} = 0.6\ V$? *(Numerical answer expected).*

(2g) *(2 points)* If the device is to be used as a lateral npn BJT in the forward active regime, what is the maximum voltage you should bias the gate relative to the source (V_{GS})? Explain. *(Numerical answer and suitable explanation expected).*

(2i) *(2 points)* If the device is to be used as an n-channel MOSFET in the saturation regime, what is the maximum voltage you should bias the body relative to the source (V_{BS})? Explain. *(Numerical answer and suitable explanation expected).*

3. *(23 points)* Consider the following amplifier below.



These are the relevant technology parameters:

$V_{Tn} = 1.0\ V$, $\mu_n C_{ox} = 100\ \mu A/V^2$, $\lambda_n = 0.01\ V^{-1}$
$V_{Tp} = -1.0\ V$, $\mu_p C_{ox} = 50\ \mu A/V^2$, $\lambda_p = 0.01\ V^{-1}$

The sizes of the devices are as follows (first number indicates width, second number indicates length, both in microns):

M1 = M5 = M9 = 8/1
M4 = M8 = 8/1
M3 = M6 = M7 = 50/1
M2= M10 = 16/1
M11 = M12 = 25/1
M13=?

(3a) *(1 points)* In the circuit schematic above, trace the signal path from input to output? *(Neat line expected).*

(3b) *(6 points)* List the transistors that perform the following functions:

(i) Signal Amplifier: _____

(ii) Current Supply or Sink: _____

(iii) Voltage Reference: _____

(3c) *(2 points)* Determine V_{BIAS} *(Numerical answer expected).*

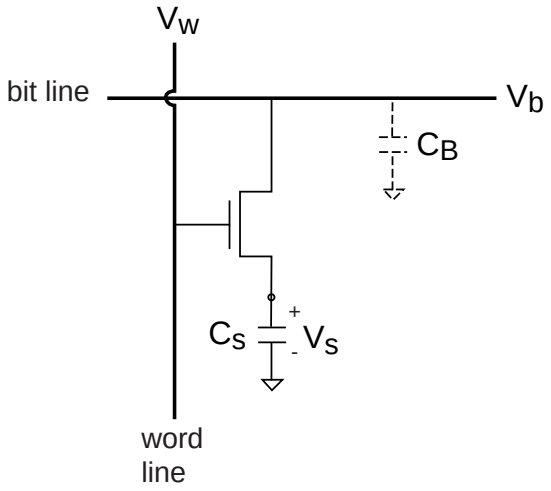
(3d) *(2 points)* If $I_O = 200\ \mu A$, what is W/L for M13? *(Numerical answer expected).*

(3e) *(4 points)* Estimate the voltage gain at point X, that is, calculate v_x/v_s.*(Numerical answer expected).*

(3f) *(4 points)* What is the output resistance of the amplifier? *(Numerical answer expected).*

(3g) *(4 points)* What are the minimum and maximum voltages that the output can swing? *(Numerical answers expected).*

4. *(28 points)* Dynamic random-access memory (DRAM) is widely used in computer applications. This is because DRAMs are relatively fast, can be made very dense and are fairly inexpensive. Consider a one-transistor (DRAM) cell sketched below:



In this DRAM cell, the information is stored in the form of charge in the capacitor C_s. If the voltage across the capacitor V_s is HI, then a "1" is stored. If V_s is LO, a "0" is stored.

The "word line" is used to select cells for reading or writing, as follows:

- if the word line is at *ground* ($V_w = 0$), the cells on that line are not selected for reading or writing;
- if the word line is at $V_w = V_{DD}$, the cells on that line are selected for reading or writing.

The "bit line" is used to write or read the bits. It has three possible states:

- if the bit line is at $V_b = V_{DD}$, a "1" is to be written
- if the bit line is at $V_b = 0\ V$, a "0" is to be written
- if the bit line is *floating*, the stored bit in the capacitor is to be read.

In this problem you will analyze the basic operation of the DRAM cell. In this DRAM cell the transistor is characterized by the following parameters: $L = 1\ \mu m$, $W = 4\ \mu m$, $\mu_n C_{ox} = 50\ \mu A/V^2$, $V_T = 1\ V$. The storage capacitor is $C_s = 50\ fF$. The bit line has a capacitance $C_B = 500\ fF$. $V_{DD} = 3.3\ V$.

□ Consider the operation of writing a "1" when the cell had a "0" stored at $t = 0^-$, that is, $V_s(t = 0^-) = 0$. At $t = 0$, the word line and the bit line are set to V_{DD} ($V_w = V_b = V_{DD}$).

(4a) *(2 points)* In what regime is the transistor operating at $t = 0^+$? Explain. *(Suitable explanation expected).*

(4b) *(2 points)* In what regime is the transistor operating at $t \to \infty$? Explain. *(Suitable explanation expected).*

(4c) *(4 points)* Estimate the value of V_s at $t \to \infty$. Explain your result. *(Numerical answer and suitable explanation expected).*

(4d) *(4 points)* Estimate the charge in C_s at $t \to \infty$. *(Numerical answer expected).*

(4e) *(4 points)* Estimate the time that it takes for the capacitor to charge up to 80% of its final value. *(Numerical answer expected).*

□ Now consider the operation of writing a "0" when the cell stored a "1" at $t = 0^-$, that is, $V_s(t = 0^-) = V_s(HI)$ from previous part (if you didn't solve for (4c), assume that $V_s(HI) = V_{DD}$). At $t = 0$, the word line is set to V_{DD} ($V_w = V_{DD}$) and the bit line is set to zero ($V_b = 0$).

(4f) *(2 points)* In what regime is the transistor operating at $t = 0^+$? Explain. *(Suitable explanation expected).*

(4g) *(2 points)* In what regime is the transistor operating at $t \to \infty$? Explain. *(Suitable explanation expected).*

□ Now consider the operation of reading a "1". In this case, again, $V_s(t = 0^-) = V_s(HI)$ (if you didn't solve for (4c), assume that $V_s(HI) = V_{DD}$). At $t = 0$, the word line is set to V_{DD} ($V_w = V_{DD}$) and the bit line is left floating with an initial value $V_b(t = 0^-) = 0$.

(4h) *(2 points)* In what regime is the transistor operating at $t = 0^+$? Explain. *(Suitable explanation expected).*

(4i) *(2 points)* In what regime is the transistor operating at $t \to \infty$? Explain. *(Suitable explanation expected).*

(4j) *(4 points)* Estimate the value of $V_b(t \to \infty)$. *(Numerical answer expected).*