# 6.012 Electronic Devices and Circuits
## Spring 2005

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**May 16, 2005**
**Final Exam**
**(200 points)**
**-OPEN BOOK-**

| | Problem |
|---|---|
| NAME_____ | 1_____ |
| RECITATION TIME_____ | 2_____ |
| | 3_____ |
| | 4_____ |
| | 5_____ |
| | Total_____ |

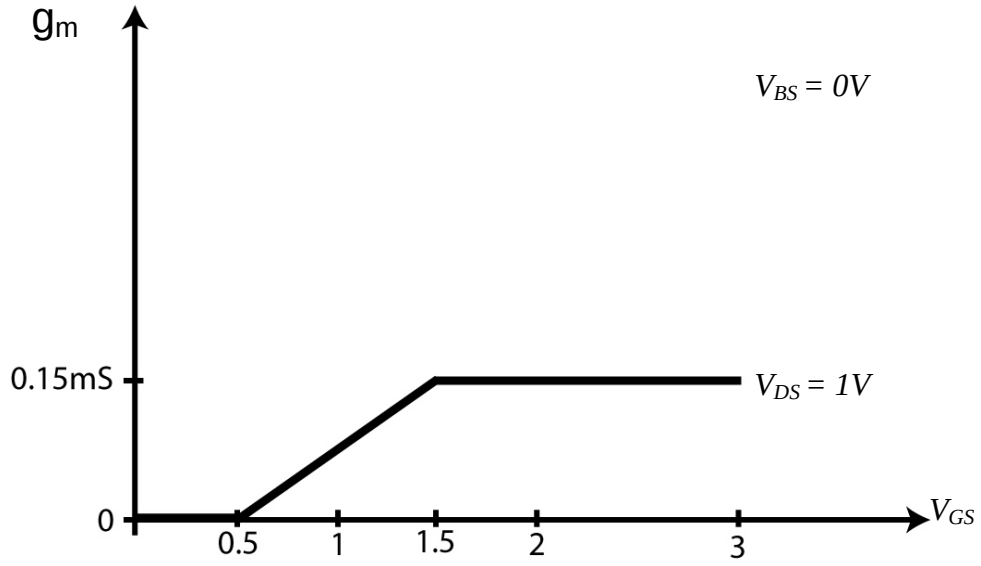
General guidelines (please read carefully before starting):

- Make sure to write your name on the space provided above.
- All answers should be given in the space provided. Please do not turn in any extra material. If you need more space, use the back page.
- You have 180 minutes to complete the quiz.
- Where required, make reasonable approximations and *state them.*
- Partial credit will be given for setting up problems without calculations. NO credit will be given for answers without reasons.
- Use the symbols utilized in class for the various physical parameters, i.e. $N_d$, $n_o$, etc.
- Every numerical answer must have the proper units next to it. Points will be subtracted for answers without units or with wrong units.
- Use the following fundamental constants and physical parameters for silicon at room temperature.

$n_i = 1.0 \times 10^{10} cm^{-3}$
$kT/q = 0.025V$
$q = 1.6 \times 10^{-19} C$
$\varepsilon_S = 1.0 \times 10^{-12} F/cm$
$\varepsilon_{OX} = 3.45 \times 10^{-13} F/cm$

**Problem 1 [40 points]**

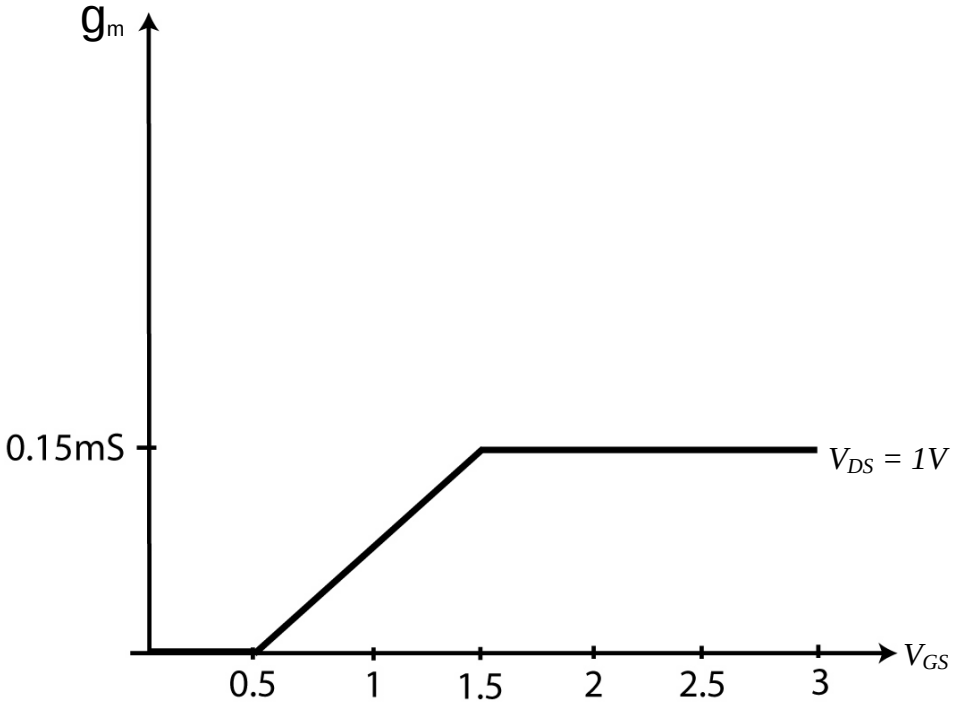
An ideal n-MOSFET has transconductance, $g_m$ characteristics as shown below:




In addition, $C_g$ is measured to be 0.1725pF at $V_{DS} = 0V$, $V_{GS} = 3V$, $V_{BS} = 0V$.

$W = 10\mu m$ and $L = 5\mu m$. Neglect channel length modulation and neglect any overlap capacitances. Assume $N_a = 10^{17}cm^{-3}$.

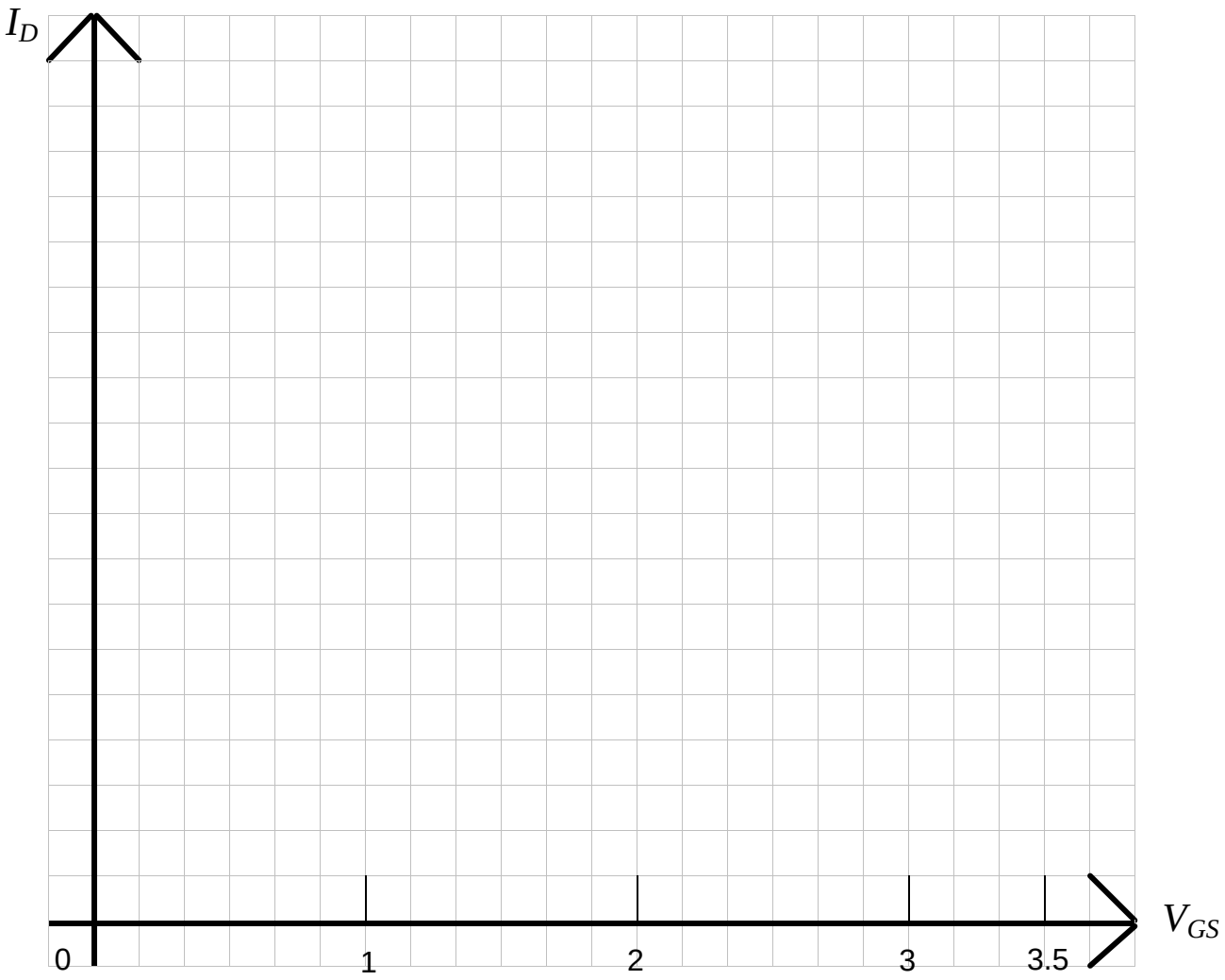
a) On the axes below, draw the $g_m$ characteristic for $V_{DS} = 2V$ and $V_{BS} = 0V$. Label the various regions of operation and any break-points on the plot.



b) Find the oxide thickness, $t_{ox}$.

c) Find the electron mobility, $\mu_n$.

d) On the axes below, sketch $I_D$ vs. $V_{GS}$ for $V_{DS} = 1V$, $V_{BS} = -3.0V$. Label the regions of operation of the device, and the value of $I_D$ at $V_{GS} = 3V$.



e) Another n-MOSFET is now fabricated with the same $W$, $L$, and $N_a$. A new gate dielectric material is used, with dielectric constant $\varepsilon_{new} = 2 \cdot \varepsilon_{ox}$, and thickness $t_{new} = 2t_{ox}$. The electron mobility for the device with the new gate dielectric is half that of a MOSFET fabricated with silicon dioxide, i.e. $\mu_{new} = 1/2\ \mu_n(oxide)$. For each of the following, assume the same bias for each device, and circle one of the choices, giving a brief justification:

i) $V_T$ for the new device, relative to the oxide-dielectric device is:

lower higher the same

ii) $g_{msat}$ for the new MOSFET, relative to the oxide-dielectric device is:

lower higher the same

iii) $g_{mb}$ for the new MOSFET, relative to the oxide-dielectric device is:

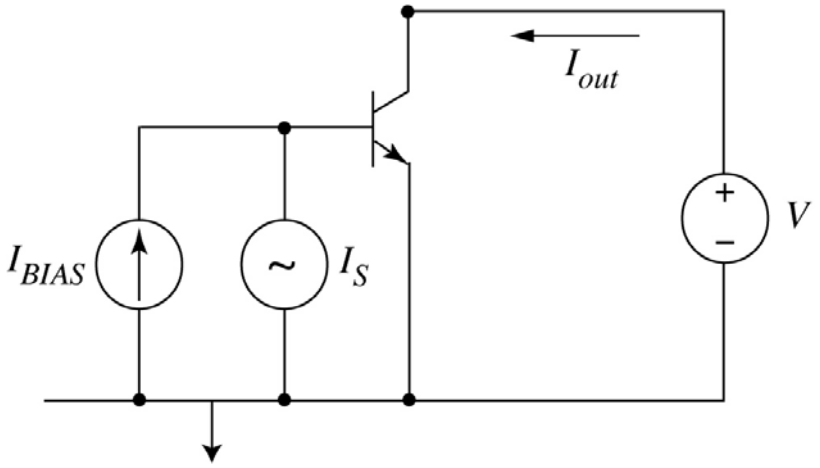
lower higher the same

iv) $C_g$ for $V_{GS} = 0V$ and $V_{DS} = 0V$ for the new device, relative to the oxide-dielectric device is:

lower higher the same

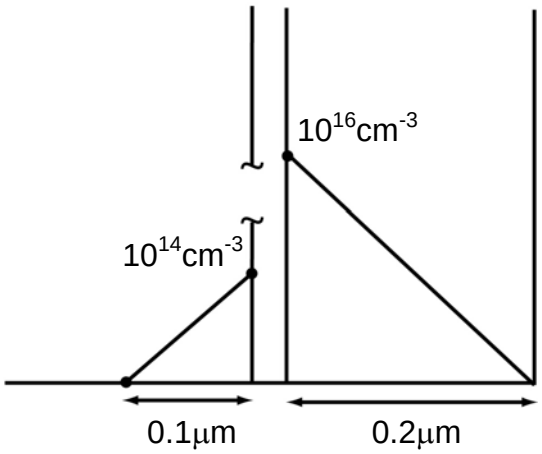
**Problem 2 [40 Points]**

A Bipolar transistor is biased to form a simple current amplifier. We are assuming no loading $(R_S \to \infty\,,\ R_L \to 0)$ as shown below:




The minority carrier concentration profiles are shown on a linear scale at the DC operating point.

$A_e$ = 10μm x 10μm
$D_n$ = 10cm$^2$/s
$D_p$ = 5cm$^2$/s

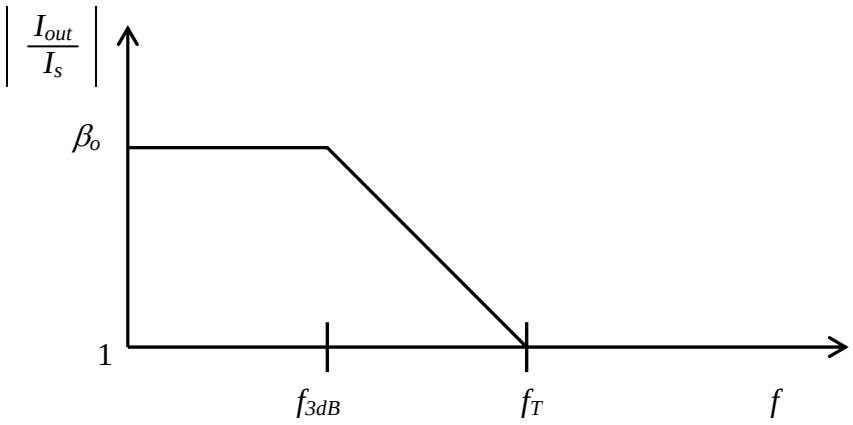



a) From the information given above, calculate $I_{BIAS}$.

b) Calculate the DC collector current $I_C$.

c) Assuming the depletion capacitances, $C_{je}$ and $C_{bc}$ are negligible, find the frequency at which the magnitude of the current gain is unity, $f = f_T$.

d) From the information given, find $\beta_o$ and $f_{3dB}$ for the Bode Plot shown below.



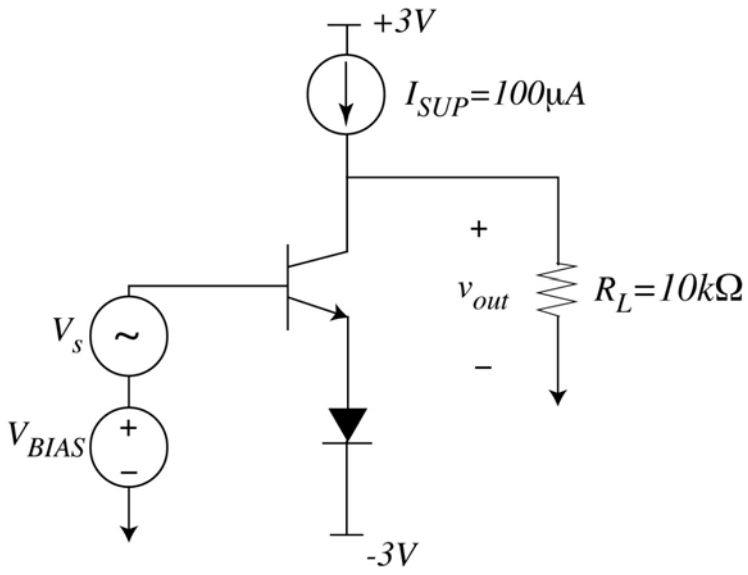

e) Given an input signal in the time domain

$$i_S(t) = 1\mu A\left( COS\left(2\pi\left(\frac{f_T}{10}\right)\right)\ t \right)$$

calculate the amplitude of the sinusoid at the output.

**Problem 3 [40 Points]**

Consider the following amplifier circuit:




*Bipolar Device Data*
$I_S = 10^{-15}A$
$\beta_o = 100$
$|V_A| \rightarrow \infty$ $(r_o \rightarrow \infty)$
$C_\pi = 200fF$
$C_\mu = 20fF$

*Diode Device Data*
$I_o = 10^{-16}A$

a) Determine $V_{BIAS}$ such that $V_{OUT}$ = 0 when $V_S$ = 0V. Assume the BJT is in the forward active region and ignore base current for this calculation.

b) Sketch an appropriate small signal model to determine the overall low frequency gain including $R_L$.

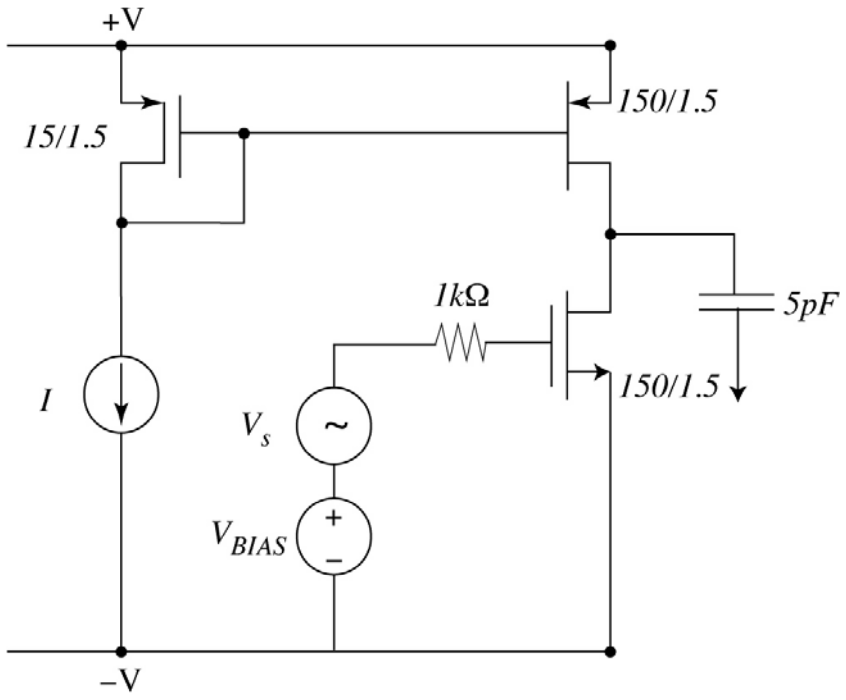
c) Calculate the overall low frequency voltage gain using the model you sketched in part (b). State any simplifying assumptions.

d) Sketch a small signal model that includes $C_\pi$and $C\mu$.

e) Using the Miller Theorem, calculate the Miller capacitance numerical value.

**Problem 4 [40 Points]**

You are given a CS amplifier driving a purely capacitive load as shown below with the NMOS and PMOS device data. Assume all transistors are in the saturated region and assume all sources are shorted to the backgate.




*Device Data*
$V_{tn} = 0.5V$
$V_{tp} = -0.5V$
$\mu_n C_{ox} = 50\mu A/V^2$
$\mu_p C_{ox} = 25\mu A/V^2$
*For W/L = 150/1.5*
$C_{gd} = 150fF$
$C_{gs} = 350fF$

Neglect channel length modulation for part a & b.

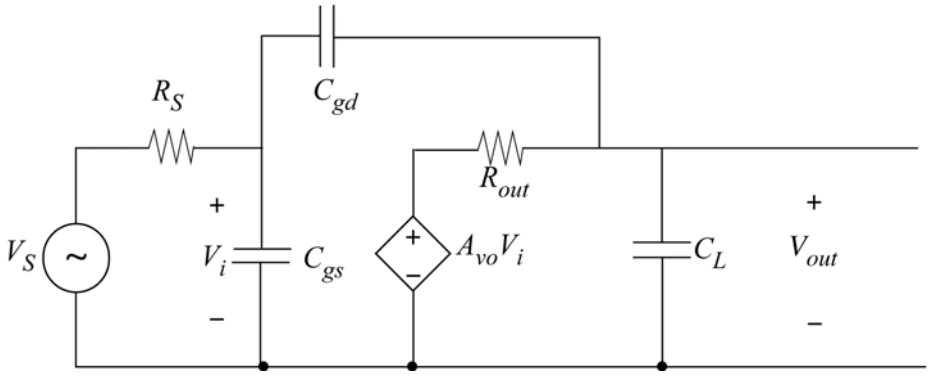
a) Calculate the value of $I$ to make the p-channel supply current source for the CS amplifier have a value of $100\mu A$.

b) Calculate $V_{BIAS}$ such that the NMOS drain current is equal to $I_{SUP} = 100\ \mu A$.

c) Calculate the transconductance of the CS amplifier at the operating point set in a & b.

d) Given that the low frequency voltage gain is –50, calculate $R_{out}$ and $(\lambda_n + \lambda_p)$. Do not assume any particular $\lambda$.

e) A two-port model for the CS amplifier with capacitors added is shown below. Using the Miller Theorem and Method of Open Circuit Time Constants, find $\omega_{3dB}$.

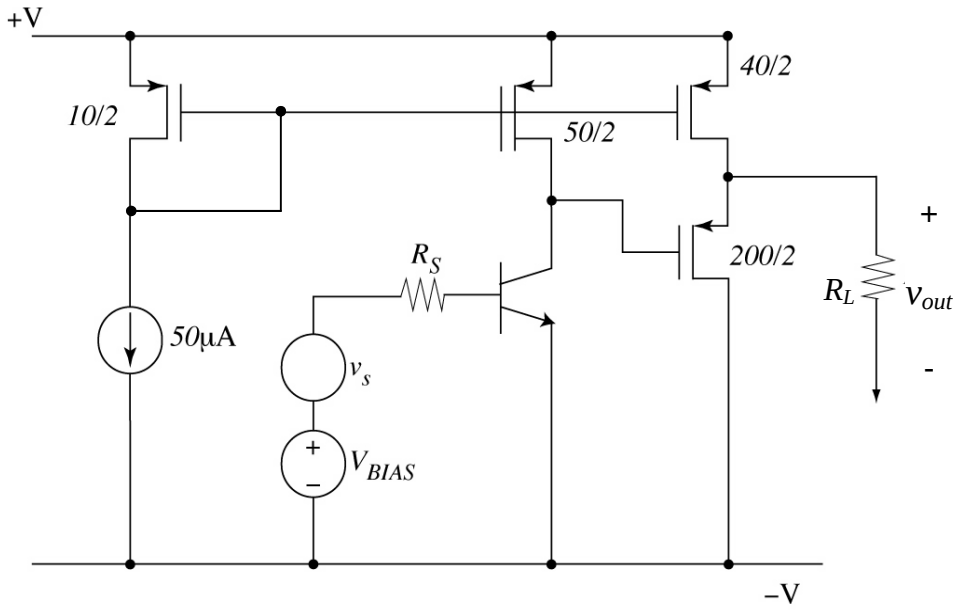


f) The width of the p-channel supply current source in the CS amplifier is reduced from $150\mu m$ to $1.5\mu m$ and the reference current source value remains $\mathrm{I}$. Estimate the new low frequency voltage gain.

g) Estimate the new $\omega_{3dB}$ with the smaller ($1.5\mu m$) p-channel current source. State assumptions to reduce the amount of work you do for this part.

**Problem 5 [40 Points]**

You are given a multistage voltage amplifier shown below. Assume that all devices are in their constant current region (MOS-saturated, BJT-forward active), at the operating point set by $V_{BIAS}$. Assume all substrates are shorted to their source.

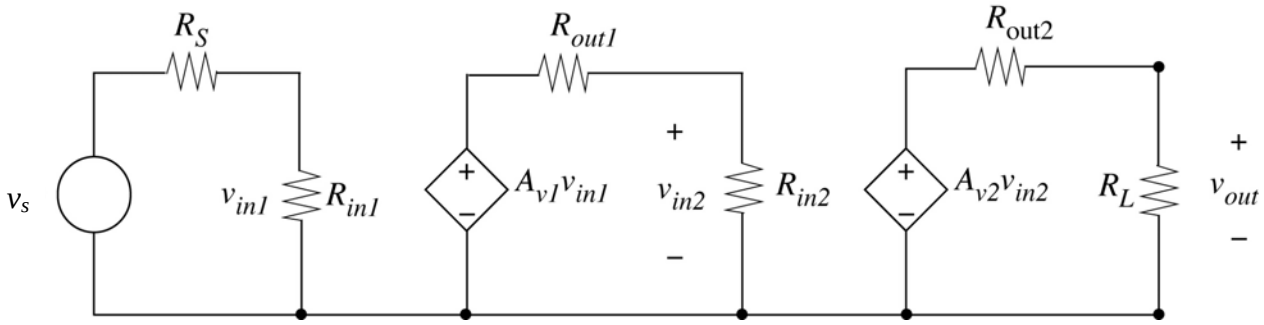



*Device Data*

$V_{Tp} = -0.5$
$\mu_p C_{ox} = 25\mu A/V^2$
$\lambda_P = 0$
$ß_o = 100$
$V_A = 10V$

a) Identify the type of stage (e.g. CS, CD) and the numerical value of the supply current sources for stages 1 and 2.

b) A small signal two-port model of both stages including $R_S$ and $R_L$ is shown below. Calculate $R_{in1}$, $A_{v1}$, and $R_{out1}$



c) Calculate $R_{in2}$, $A_{v2}$, and $R_{out2}$.

d) Given $R_S = 20k\Omega$, adjust the width of the p-channel stage 1 supply current source such that 50% of the voltage enters the amplifier.

e) Given $R_L = 500\Omega$ adjust the width of the p-channel stage 2 supply current source such that 50% of the voltage is transferred to the load.

f) What is the overall voltage gain $v_{out}/v_s$ [assuming the p-channel current sources are sized as in (d) and (e) above]?

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