# Part 5. Field Effect Transistors

Field Effect transistors (FETs) are the backbone of the electronics industry. The remarkable progress of electronics over the last few decades is due in large part to advances in FET technology, especially their miniaturization, which has improved speed, decreased power consumption and enabled the fabrication of more complex circuits. Consequently, engineers have worked to roughly double the number of FETs in a complex chip such as an integrated circuit every 1.5-2 years; see Fig. 1 in the Introduction. This trend, known now as Moore's law, was first noted in 1965 by Gordon Moore, an Intel engineer. We will address Moore's law and its limits specifically at the end of the class. But for now, we simply note that FETs are already small and getting smaller. Intel's latest processors have a source-drain separation of approximately 65nm.

In this section we will first look at the simplest FETs: molecular field effect transistors. We will use these devices to explain field effect switching. Then, we will consider ballistic quantum wire FETs, ballistic quantum well FETs and ultimately non-ballistic macroscopic FETs.

### (i) Molecular FETs

The architecture of a molecular field effect transistor is shown in Fig. 5.1. The molecule bridges the source and drain contact providing a *channel* for electrons to flow. There is also a third terminal positioned close to the conductor. This contact is known as the *gate*, as it is intended to control the flow of charge through the channel. The gate does not inject charge directly. Rather it is capacitively coupled to the channel; it forms one plate of a capacitor, and the channel is the other. In between the channel and the conductor, there is a thin insulating film, sometimes described as the 'oxide' layer, since in silicon FETs the gate insulator is made from $SiO_2$. In the device of Fig. 5.1, the gate insulator is air.

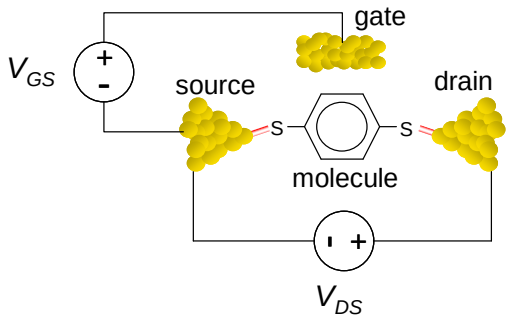



**Fig. 5.1.** A molecular FET. An insulator separates the gate from the molecule. The gate is not designed to inject charge. Rather it influences the molecule's potential.

# Part 5. Field Effect Transistors

## FET switching

In digital circuits, an ideal FET has two states, ON and OFF, selected by the potential applied to the gate. In the OFF state, the channel is closed to the flow of electrons even if a bias is applied between the source and drain electrodes. To close the channel, the gate must prevent the injection of electrons from the source. For example, consider the molecular FET in Fig. 5.2. Here, we follow FET convention and measure all potentials relative to a grounded source contact. For a gate bias of $V_{GS}$ < ~6.2V little current flows through the molecule. But for ~6.2V< $V_{GS}$ < ~6.4V the FET is ON and the channel is conductive.

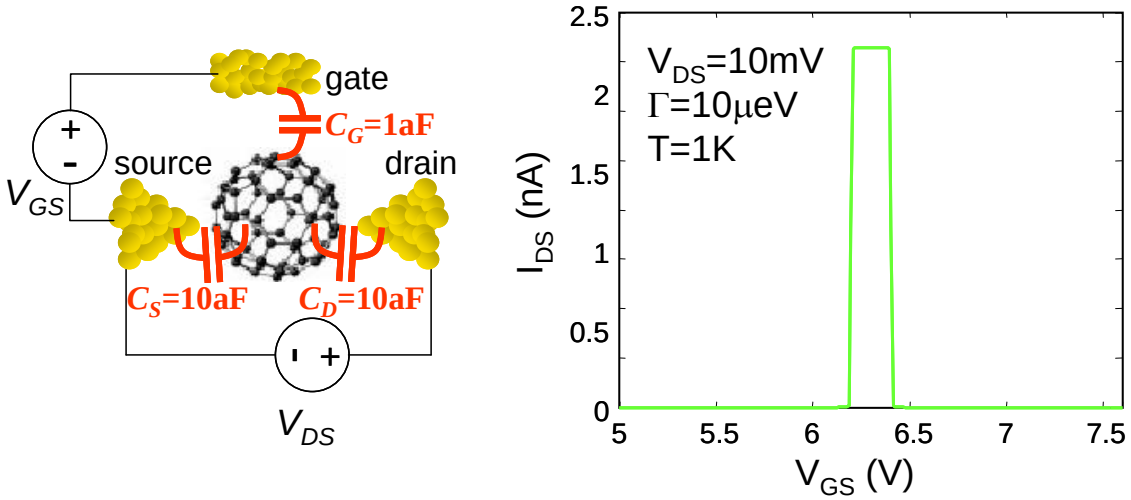



**Fig. 5.2.** The $I_{DS}$-$V_{GS}$ characteristics of a FET employing the buckyball molecule C60. At equilibrium the source and drain chemical potentials are at -5eV, and the molecule's LUMO is at -4.7eV. The various electrostatic capacitances in the device are labeled. As the gate potential is increased, the LUMO is pushed lower. At approximately $V_{GS}$ = 6.3V, it is pushed into resonance with the source and drain contacts and the current increases dramatically. The width of the LUMO determines the sharpness of the resonance. Note 'aF' is the symbol for atto Farad ($10^{-18}$ F).

As shown in Fig. 5.3, the transitions are much more gradual if the molecular energy level is broader. Similarly, increasing the temperature can also blur the switching characteristics.

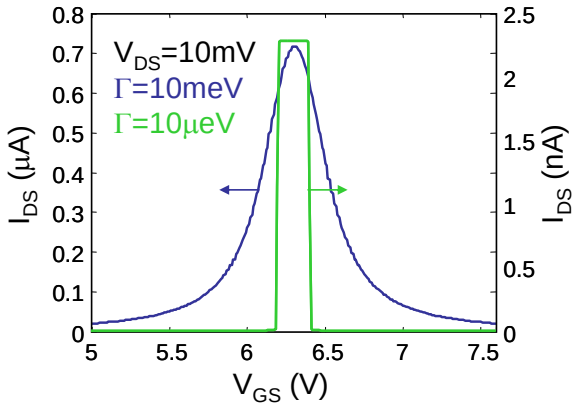



**Fig. 5.3.** A comparison between the switching characteristics of molecular FETs with broad and narrow energy levels. Note the different current scales.

The origin of FET switching is explained in Fig. 5.4. The gate potential acts to shift energy levels in the molecule relative to the contact chemical potentials. When an energy level is pushed between $\mu_1$ and $\mu_2$ electrons can be injected from the source. Correspondingly, the current is observed to increase. Further increases in gate potential push the energy level out of resonance and the current decreases again at ~ 6.4V.

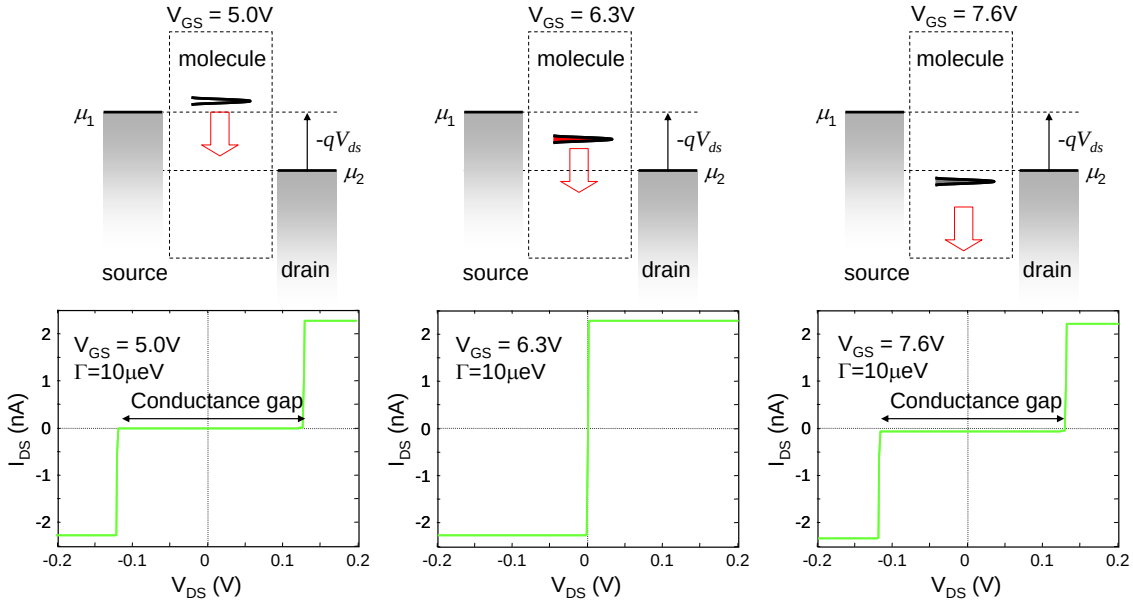



**Fig. 5.4.** The $I_{DS}$-$V_{DS}$ characteristics of the FET from Fig. 5.2. Outside resonance a conductance gap opens because additional source-drain bias is required to pull the molecular level between the source and drain chemical potentials.

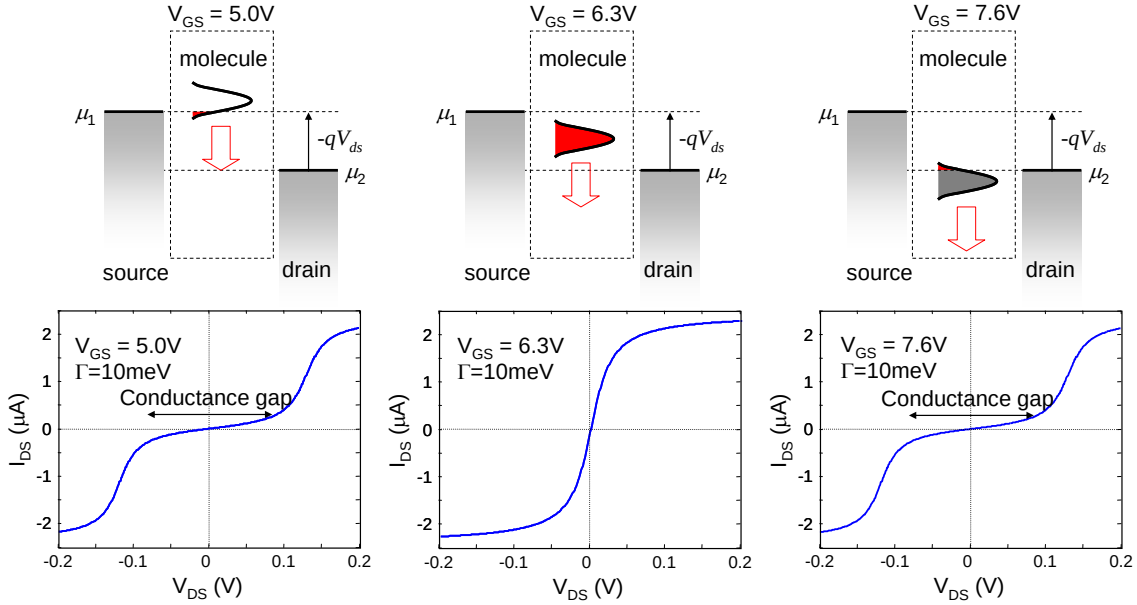



**Fig. 5.5.** The $I_{DS}$-$V_{DS}$ characteristics of the FET from Fig. 5.2, except this time the width of the LUMO is 1000 x broader in energy. The corresponding IV shows more gradual transitions, a narrower conductance gap and much higher currents.

# Part 5. Field Effect Transistors

## FET Calculations

Unlike the two terminal case, where we arbitrarily set $E_F = 0$ and shifted the Source and Drain potentials under bias, the FET convention fixes the Source electrode at ground. There are two voltage sources: $V_{GS}$, the gate potential, and $V_{DS}$, the drain potential. We analyze the influence of $V_{GS}$ and $V_{DS}$ on the molecular potential using capacitive dividers and superposition:

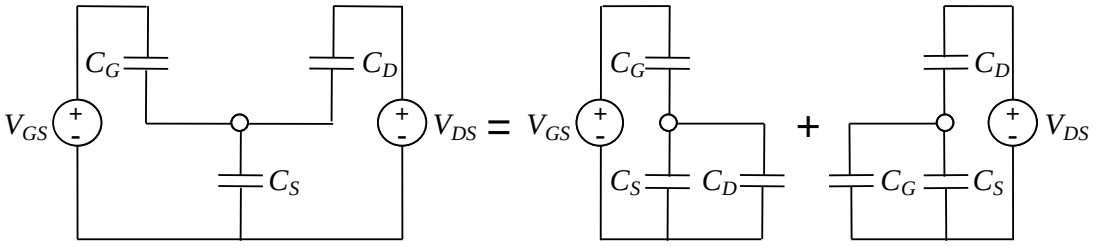



**Fig. 5.6.** Analyzing a molecular FET using a capacitive divider and superposition.

$$U_{ES} = -qV_{GS}\frac{1/(C_D + C_S)}{1/(C_D + C_S) + 1/C_G} - qV_{DS}\frac{1/(C_G + C_S)}{1/(C_G + C_S) + 1/C_D} \tag{5.1}$$

Simplifying, and noting that the total capacitance at the molecule is $C_{ES} = C_S + C_D + C_G$:

$$U_{ES} = -qV_{GS}\frac{C_G}{C_{ES}} - qV_{DS}\frac{C_D}{C_{ES}} \tag{5.2}$$

We also must consider charging. As before,

$$U_C = \frac{q^2}{C_{ES}}(N - N_0) \tag{5.3}$$

Recall that charging opposes shifts in the potential due to $V_{GS}$ or $V_{DS}$. Thus, if charging is significant, the switching voltage increases; see Fig. 5.7.

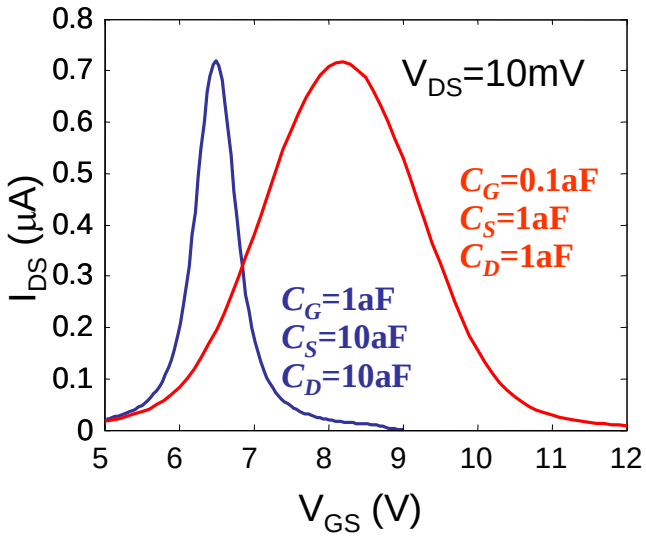



**Fig. 5.7.** $I_{DS}$-$V_{GS}$ characteristics for the FET of Fig. 5.2 calculated under two different sets of capacitances. Charging is more important for the smaller capacitances. The switching voltage for this device is observed to increase to ~ 8.1V.

Adding the static potential due to $V_{DS}$ and $V_{GS}$ gives, the potential $U$ in terms of the charge, $N$, and bias

$$U = -qV_{GS}\frac{C_G}{C_{ES}} - qV_{DS}\frac{C_D}{C_{ES}} + \frac{q^2}{C_{ES}}\left(N - N_0\right) \tag{5.4}$$

We also have an expression for potential for $N$ in terms of $U$ (see Eq. (3.31))

$$N = \int_{-\infty}^{\infty} g\left(E-U\right)\frac{\tau_D f\left(E,\mu_S\right)+\tau_S f\left(E,\mu_D\right)}{\tau_S+\tau_D}dE \tag{5.5}$$

As before, Eqns. (5.4) and (5.5) must typically be solved iteratively to obtain $U$. Then we can solve for the current using:

$$I = q\int_{-\infty}^{\infty} g\left(E-U\right)\frac{1}{\tau_S+\tau_D}\left(f\left(E,\mu_S\right)-f\left(E,\mu_D\right)\right)dE \tag{5.6}$$

**Quantum Capacitance in FETs**

Unfortunately, Eqns. (5.4) and (5.5) typically must be solved iteratively. But insight can be gained by studying a FET with a few approximations.

Another way to think about charging is to consider the effect on the channel potential of incremental changes in $V_{GS}$ or $V_{DS}$. We can then apply simple capacitor models of channel charging to determine the channel potential in Eq. (5.6).

If the potential in the channel changes by $\delta U$ then the number of charges in the channel changes by

$$\delta N = -g\left(E_F\right)\delta U \tag{5.7}$$

Note that we have assumed $T$ = 0K, and note also the negative sign – making the channel potential more negative increases the number of charges.

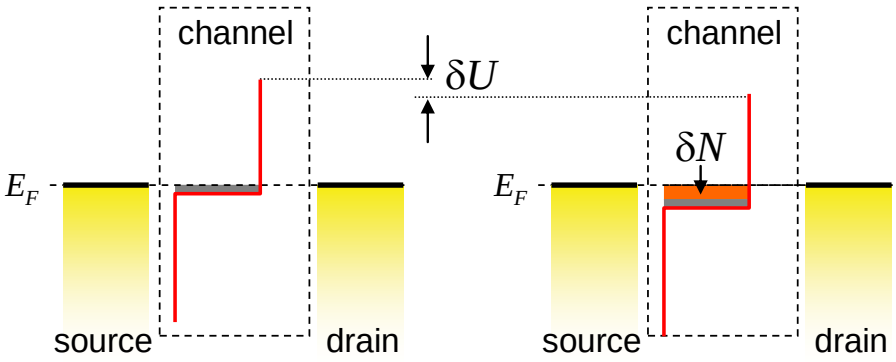



**Fig. 5.8.** A shift in the channel potential changes the number of charges in the channel.

Substituting back into Eq. (5.4) gives

$$\delta U = -q\delta V_{GS}\frac{C_G}{C_{ES}} - q\delta V_{DS}\frac{C_D}{C_{ES}} - \frac{q^2}{C_{ES}}g\left(E_F\right)\delta U \tag{5.8}$$

Collecting $\delta U$ terms gives

$$\delta U = -q\delta V_{GS}\frac{C_G}{C_{ES}+C_Q} - q\delta V_{DS}\frac{C_D}{C_{ES}+C_Q} \tag{5.9}$$

Where we recall the **quantum capacitance** ($C_Q$):

$$C_Q = q^2 g\left(E_F\right) \tag{5.10}$$

Using the quantum capacitance, we can easily construct a small signal model for changes in $V_{GS}$ or $V_{DS}$. See, for example the small signal $V_{GS}$ model in Fig. 5.9. Note that the value of the quantum capacitance depends on the channel potential at the bias point.

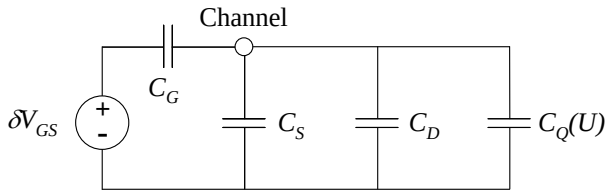



**Fig. 5.9.** A small signal model for the channel potential.

Using Eq. (5.7) we can also determine a small signal model for the charge in the channel.

$$q\delta N = \delta V_{GS}\frac{C_G C_Q}{C_{ES}+C_Q} \tag{5.11}$$

In the next section we will consider FET operation under two limiting cases: (i) when $C_Q$ is large relative to $C_{ES}$, and (ii) when $C_Q$ is small. The two cases typically correspond to the ON and OFF states of a FET, respectively.

**Simplified models of FET switching**

To further simplify the problem, we define two quantities, $N_S$ and $N_D$, the charges injected into the channel from the source and drain contacts, respectively. Next, we assume that $\tau = \tau_S + \tau_D$, where $\tau_S = \tau_D$ and $C_G >> C_S$, $C_D$, Eqs (5.4), (5.5) and (5.6)become

$$U = -qV_{GS} + \frac{q^2}{C_G}\left(N - N_0\right) \tag{5.12}$$

$$N = \frac{N_S + N_D}{2} \tag{5.13}$$

$$I = \frac{q}{\tau}\left(N_S - N_D\right) \tag{5.14}$$

where

$$N_S = \int_{-\infty}^{\infty} g\left(E-U\right) f\left(E,\mu_S\right)dE \tag{5.15}$$

$$N_D = \int_{-\infty}^{+\infty} g\left(E-U\right) f\left(E,\mu_D\right)dE \tag{5.16}$$

Conduction in the FET is controlled by the number of electron states available to charges injected from the source. For switching applications, transistors must have an OFF state

where $I_{DS}$ is ideally forced to zero. The OFF state is realized by minimizing the number of empty states in the channel accessible to electrons from the source. In the limit that there are no available states, the channel is a perfect insulator.

Switching between ON and OFF states is achieved by using the gate to push empty channel states towards the source chemical potential. The transition between ON and OFF states is known as the threshold. Although the transition is not sharp in every channel material, it is convenient to define a gate bias known as the *threshold voltage*, $V_T$, where the density of states at the source chemical potential $g(E_F)$ undergoes a transition.

**The Zero Charging limit**

As we saw in Part 3, charging-induced shifts in the energy levels of conductors can significantly complicate the calculation of *IV* characteristics. Equation (5.11) demonstrates that charging can be neglected if the quantum capacitance is much smaller than the electrostatic capacitance, *i.e.* $C_Q << C_{ES}$. For example, in Eq. (5.11), if $C_Q << C_{ES}$ then the charging, $\delta N \rightarrow 0$.

In the zero charging limit, Eq. (5.12) reduces to

$$U = -qV_{GS} \tag{5.17}$$

*i.e.* in this limit the channel potential simply tracks the gate bias.

Thus, in the zero charging limit, we can determine the current directly from Eq. (5.6), with the channel potential $U = -qV_{GS}$.

The zero charging limit almost always holds for insulators and transistors in the OFF state because the density of states at the Fermi level is small in both these examples. Determining whether a transistor remains in the zero charging limit in the ON state requires a comparison of $C_Q$ and $C_{ES}$. Bulk devices very rarely operate within the zero charging limit in the ON state. But many small conductors contain relatively few states at the Fermi level even in the ON state, such that $C_Q << C_{ES}$ even when significant channel current is flowing.

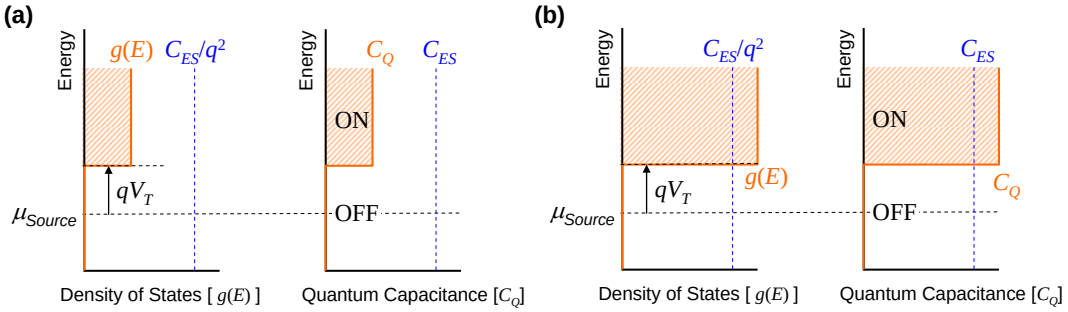



**Fig. 5.10.** We consider a channel material with a sharp transition in its density of states. In **(a)** we show a channel which remains in the insulator limit even in the ON regime. In **(b)** the channel states have sufficient density for the channel to be metallic in the ON regime.

### The Strong Charging Limit

In metals and many large transistors in the ON state, the density of states at the Fermi level is sufficiently large that adding charges barely moves the channel potential. We say that the Fermi level is *pinned*. In the limit that $g(E_F) \rightarrow \infty$ then $\Delta U \rightarrow 0$.

In terms of the quantum capacitance, we find that if $C_Q >> C_{ES}$, Eq. (5.11) reduces to

$$q\delta N = \delta V_{GS} C_G \tag{5.18}$$

This limit is also known as **strong inversion** in conventional FET analysis. The channel transforms from an insulator to a metal. The transition occurs when the gate bias equals the threshold voltage, $V_T$, which is defined as the gate bias required to push the channel energy level down to the source workfunction.

In the strong charging/metallic limit, the gate and channel act as two plates of a capacitor. The charge in the channel then changes linearly with additional gate bias. In FETs, the channel potential relative to the source, $V(x)$, may also vary with position. Including the channel potential and the threshold voltage in Eq. (5.18) yields:

$$qN = C_G \left( V_{GS} - V_T - V(x) \right) \tag{5.19}$$

One way to interpret the metallic limit is to consider the difference between the actual position of the conduction band edge and its position in the absence of charging. The difference is proportional to the amount of charging; see Fig. 5.11. Note that the shaded region in the figure does not represent filled electron states below the conduction band. These electrons are in fact all at the bottom of the conduction band. Rather this the same graphical tool that we used in Part 3 to analyze charging within conductors.

The metallic or strong inversion limit is only maintained for $V_{GS} - V_T - V(x) > 0$. If $V(x)$ crosses the zero charging limit ($V_{GS}$-$V_T$) then charging decreases to zero. This is known as 'pinch off'.

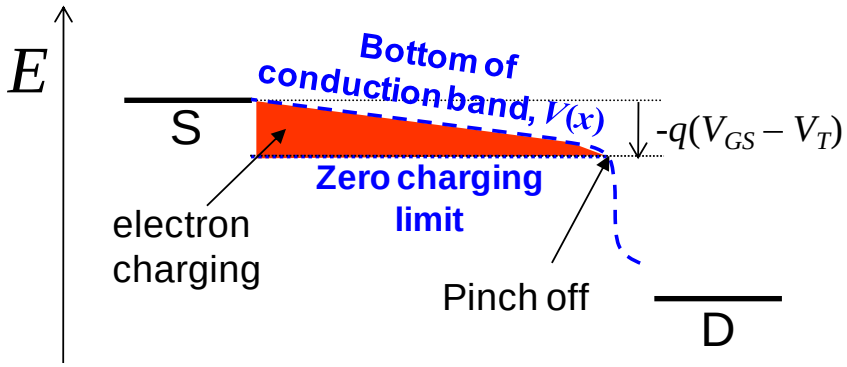



**Fig. 5.11.** Charging opposes gate-induced changes in the channel potential. Here we illustrate the effect of charging in a non-ballistic FET. In the absence of charging, increasing gate potential lowers the conduction band edge (the 'zero charging limit'). Charging pushes the conduction band edge back up towards the source workfunction. The red shaded region is the difference between the actual channel potential and the zero charging limit. It represents the population of electrons in the conduction band. It does not represent filled states below the bottom of the conduction band.

**The temperature dependence of current in the OFF state**

Both nanoscale and larger transistors have a small quantum capacitance in the OFF state, which is also known as subthreshold since $V_{GS} < V_T$.

But even if the density of states is zero between $\mu_S > E > \mu_D$, at higher temperatures, some electrons may be excited into empty states well above the Fermi Energy. If the density of states is very low at the Fermi Energy, but higher far from the Fermi level, then we can model the Fermi distribution by an exponential tail. Recall that this is known as a non-degenerate distribution; see Fig. 5.12.

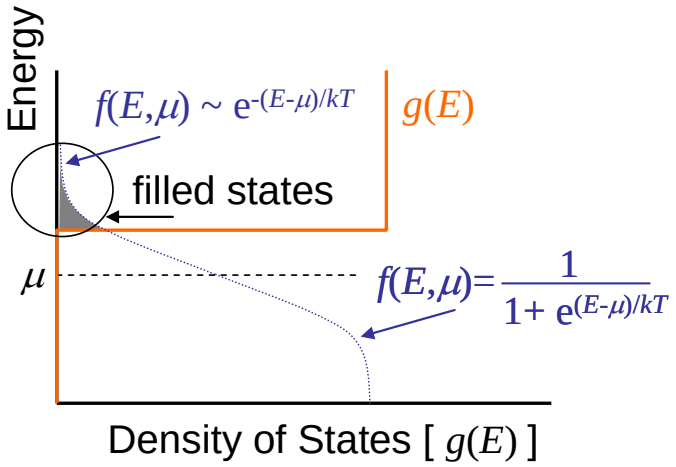



**Fig. 5.12.** If only the extreme tail states of the Fermi distribution are filled, then we can model the distribution by an exponential. This is common when the density of states at the Fermi Energy is small.

Equation (5.14) becomes

$$N_S = \int_{-\infty}^{\infty} g(E-U)\, e^{-(E-\mu_S)/kT}\, dE \tag{5.20}$$

Now changing the variable of integration to $E' = E - U$

$$N_S = \int_{-\infty}^{\infty} g(E')\, e^{-(E'+U-\mu_S)/kT}\, dE' \tag{5.21}$$

Simplifying

$$N_S = e^{-U/kT} \int_{-\infty}^{\infty} g(E')\, e^{-(E'-\mu_S)/kT}\, dE' \tag{5.22}$$

Similarly,

$$N_D = e^{-U/kT} \int_{-\infty}^{\infty} g(E')\, e^{-(E'-\mu_D)/kT}\, dE' \tag{5.23}$$

Thus, from Eq. (5.14) the current is

$$I = \frac{q}{\tau} \exp\left[\frac{qV_{GS}}{kT}\right] . \int_{-\infty}^{\infty} g(E') \left( e^{-(E'-\mu_S)/kT} - e^{-(E'-\mu_D)/kT} \right) dE' \tag{5.24}$$

Equation (5.24) holds in the limit that $C_G >> C_S, C_D$. In general, we find that the current in the subthreshold region is

$$I = I_0 \exp\left[\frac{qV_{GS}}{kT}\frac{C_G}{C_{ES}}\right] \tag{5.25}$$

Taking logarithm of both sides we find,

$$\log_{10} I = \frac{q}{kT}\frac{C_G}{C_{ES}}(\log_{10} e)V_{GS} + \log_{10} I_0 \tag{5.26}$$

The slope, $S$, of the subthreshold regime is usually expressed gate volts per decade of drain current. At room temperature, the optimum, when $C_G >> C_S, C_D$, is

$$S = \frac{kT}{q}\frac{1}{\log_{10} e} \approx 60 \text{ mV/decade} \tag{5.27}$$

The slope becomes much sharper at low temperatures; see Fig. 5.13.

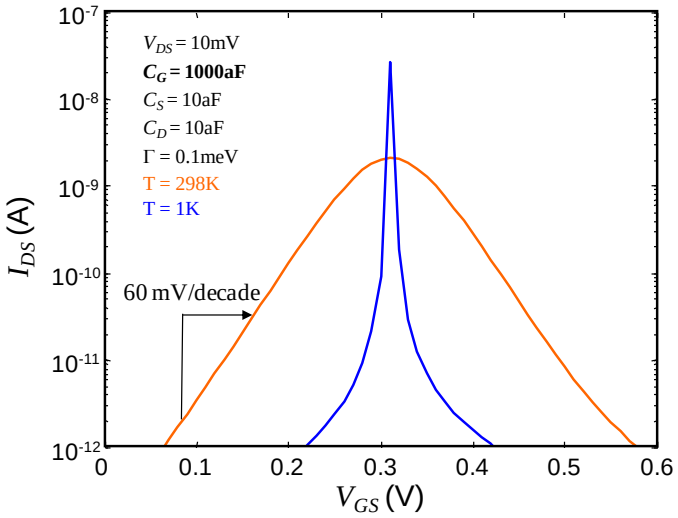



**Fig. 5.13.** A comparison of the switching characteristics of our C60 model FET at T = 1K and room temperature. In the OFF regime, the current varies exponentially with gate bias, i.e. a straight line on a log-linear plot. The slope at room temperature is 60 mV/decade of drain current.

**Transconductance**

A field effect transistor is a voltage controlled current source. Its input is the gate potential, and the output is the source-drain current. In applications, we usually desire that the FET amplifies small changes in $V_{GS}$. Thus, an important figure of merit for an FET is the transconductance, defined as

$$g_m = \frac{dI_{ds}}{dV_{gs}} \tag{5.28}$$

In the OFF state, the quantum capacitance is small and the gate's only influence on the FET is its electrostatic control of the channel potential. From Eq. (5.1), we see that this control is maximized when

$$C_G >> C_S, C_D \tag{5.29}$$

This is an important design goal for FETs. Under this limit the transconductance is commonly expressed as:

$$\frac{g_m}{I_{ds}} = \frac{1}{I_{ds}}\frac{dI_{ds}}{dV_{gs}} = \frac{q}{kT} \tag{5.30}$$

Good electrostatic control of the channel may be achieved either by increasing the dielectric constant of the gate insulator, or by reducing the thickness of the gate insulator.

A good rule of thumb is that the gate must be much closer to the channel than either the source or drain contacts. Fig. 5.14 shows the impact of varying $C_G$ on our C60 molecular transistor. Increasing $C_G$ shifts the switching gate voltage much lower.

Interestingly, to obtain this ideal characteristic, we increased $C_G$ by three orders of magnitude relative to the more practical value used originally. This corresponds to increasing dielectric constant or reducing the gate-channel separation by three orders of magnitude.

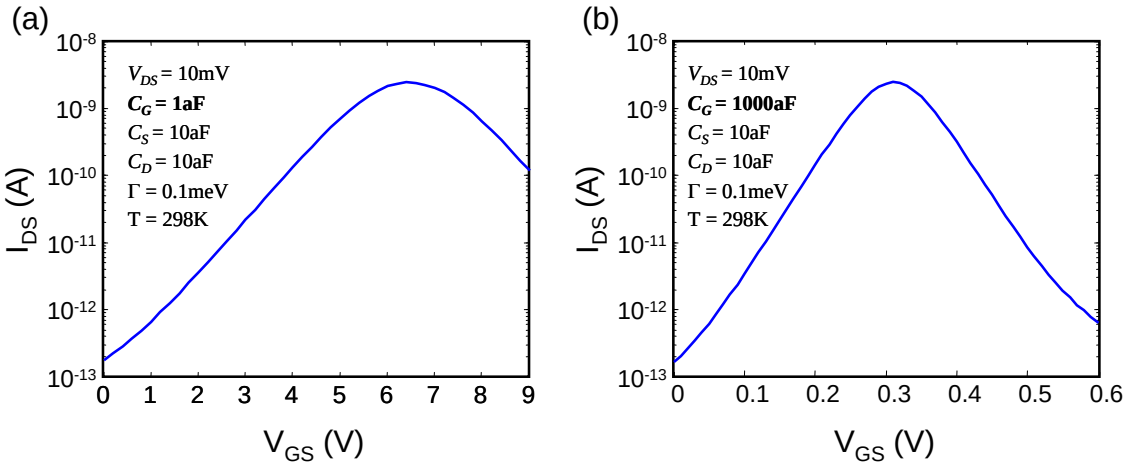



**Fig. 5.14.** A comparison of two C60 FETs. In **(a)** the gate has poor electrostatic control over the channel as evidenced by the small $C_G$. In **(b)** the control is better, and the switching voltage is much lower.

For a molecular transistor with source-drain separation of a few nanometers, the gate insulator should be only a few Ångstroms – too thin to sufficiently insulate the gate. This represents a possibly insurmountable obstacle to 0-d channel devices such as single molecule FETs.

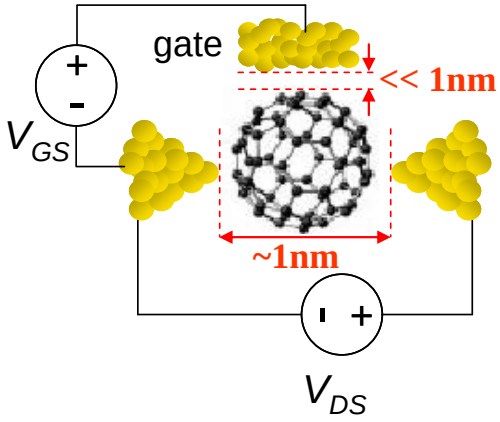



**Fig. 5.15.** For high transconductance, the gate capacitance must be much higher than the source or drain channel capacitances. This forces impractically small gate-channel separations in molecular transistors.

### (ii) 1d and 2d FETs

The central equation of conduction is

$$I = \frac{q\left(N_S - N_D\right)}{\tau} \tag{5.31}$$

In 0-d the time constant, $\tau$, was defined as the sum of the interfacial electron transfer time $\tau_S$ and $\tau_D$, which in turn can be thought of as representations of the interaction energy between the 0-d conductor and the source and drain contacts: $\tau_S = \Gamma_S/\hbar$ and $\tau_D = \Gamma_D/\hbar$, respectively.

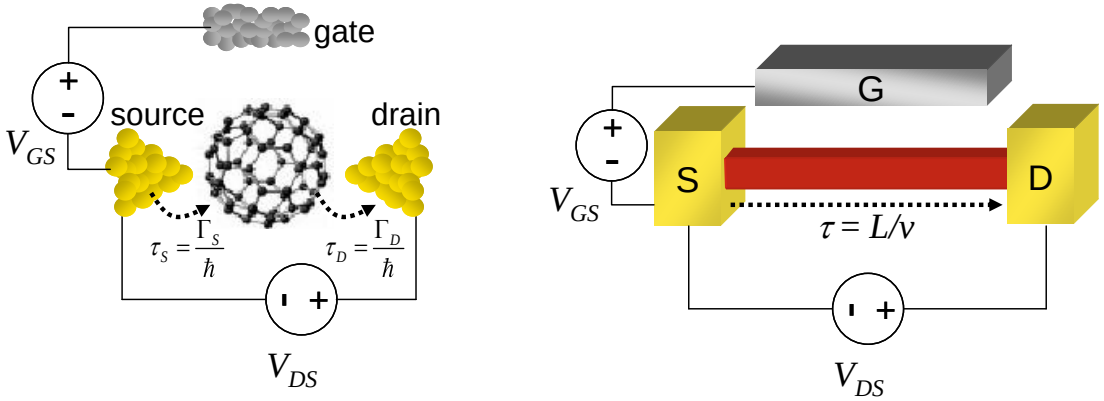



**Fig. 5.16. (a)** Electron transfer times in a 0-d conductor are related to the interaction energy $\Gamma$ between the contact and the conductor. **(b)** In higher dimensions, we must determine the transit time from the electron velocity.

In higher dimensions, however, the electron transfer times at the contacts are less important. Rather, $\tau$ is the transit time for an electron in the conductor. It is given by

$$\tau = \frac{L_x}{v_x} \tag{5.32}$$

where $L_x$ is the length of the channel, and $v_x$ is the velocity component of the electron parallel to the source-drain current. It is important to note that in 1-d, 2-d and 3-d conductors the transit time is dependent on the energy of the electron since the electron velocity, $v_x$, is dependent on energy.

The other important change from the 0-d model concerns the density of states. In 0-d all states are accessible to electrons from both the source and drain contacts. But in higher dimensional ballistic devices, electrons injected from the source are only able to access states with momenta directed away from the source. We call these $+k$ states. Similarly, the drain only injects electrons into $-k$ states. Thus, we break the dispersion relation and density of states into two pieces, the density of $+k$ states is given by $g^{+}(E)dE$ and the density of $-k$ states is given by $g^{-}(E)dE$.

To summarize, in 1-d, 2-d and 3-d the fundamental equations for a transistor are:

$$U_{ES} = -qV_{GS}\frac{C_G}{C_{ES}} - qV_{DS}\frac{C_D}{C_{ES}} + \frac{q^2}{C_{ES}}\left(N - N_0\right) \tag{5.33}$$

$$N = N_S + N_D \tag{5.34}$$

$$I = \frac{q}{\tau}\left(N_S - N_D\right) \tag{5.35}$$

where

$$N_S = \int_{-\infty}^{\infty} g^{+}\left(E - U\right) f\left(E, \mu_S\right) dE \tag{5.36}$$

$$N_D = \int_{-\infty}^{+\infty} g^{-}\left(E - U\right) f\left(E, \mu_D\right) dE \tag{5.37}$$

**The ballistic quantum wire FET.**[†]

Consider the ballistic quantum wire FET shown in Fig. 5.17.

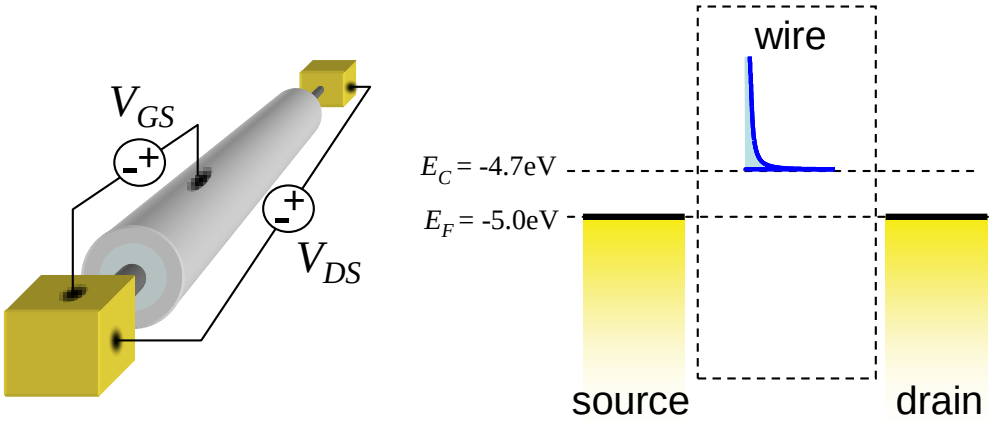



**Fig. 5.17.** A quantum wire FET. The gate is wrapped around the wire to maximize the capacitance between the channel and the gate. The length of the wire is $L$ = 100nm, the gate capacitance is $C_G$ = 50 aF per nanometer of wire length, and the electron mass, $m$, in the wire is $m = m_0$=9.1x10$^{-31}$ kg.

We will assume that there is only one parabolic band in the wire.

From Eq. (2.37), the density of states in the wire is:

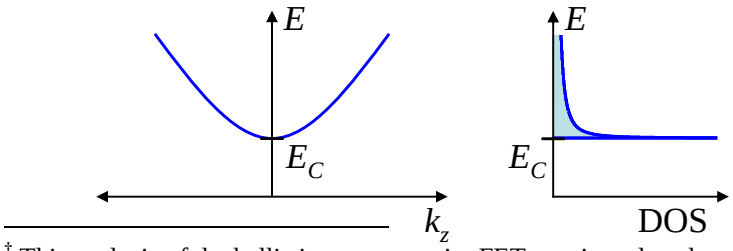



**Fig. 5.18.** The bandstructure and density of states in a single mode quantum wire.

[†] This analysis of the ballistic quantum wire FET was introduced to me by Mark Lundstrom at Purdue University. For a complete reference see Mark Lundstrom and Jing Guo, 'Nanoscale Transistors: Physics, Modeling, and Simulation', Springer, New York, 2006.

$$g(E)\,dE = \frac{2L}{h}\sqrt{\frac{2m}{E-E_C}}\,u(E-E_C)\,dE\,, \tag{5.38}$$

where $L$ is the length of the wire, and $m$ is the electron mass in the wire. But only half of these states contain electrons traveling in the positive direction. Thus, we must divide Eq. (5.38) by two to yield:

$$g^{+}(E)\,dE = \frac{1}{2}\times\frac{2L}{h}\sqrt{\frac{2m}{E-E_C}}\,u(E-E_C)\,dE \tag{5.39}$$

Given the position of the Fermi Energy, this band is the conduction band. We will label the energy at the bottom of the conduction band, $E_C$. Since we model electrons moving along the wire as plane waves, within the parabolic band we have

$$E - E_C = \frac{\hbar^2 k^2}{2m} = \frac{1}{2}mv^2 \tag{5.40}$$

We can rewrite Eq. (5.39) in terms of the velocity, $v$, of the electron:

$$g^{+}(E)\,dE = \frac{1}{2}\times\frac{4L}{hv(E)}\,u(E-E_C)\,dE \tag{5.41}$$

Now $L/v$ is the transit time of an electron through the wire, thus

$$g^{+}(E)\,dE = \frac{1}{2}\times\frac{4\tau(E)}{h}\,u(E-E_C)\,dE\,. \tag{5.42}$$

We can substitute Eq. (5.42) into the expression for the current density (Eq. (5.31)) to obtain

$$I = \frac{2q}{h}\int_{-\infty}^{+\infty} u(E-E_C-U)\left(f(E,\mu_S)-f(E,\mu_D)\right)dE\,. \tag{5.43}$$

**Quantum dot models of quantum wire transistor channels**

Under bias we expect a spatial variation in the potential along a quantum wire. Current flow may also vary the charge density along the wire, which in turn affects the potential profile. Thus, the potential variation must be determined self consistently with the current flow.

We have seen in Part 4 that the conduction band edge in a ballistic conductor is determined by the point of maximum potential in the conductor. For electrostatic purposes, we will approximate this point on the quantum wire as a quantum dot, and then employ our discrete capacitive models of potential to calculate changes in the conduction band edge.

Usually the highest potential is located next to the source, because application of forward bias at the drain pulls the potential down along the channel.

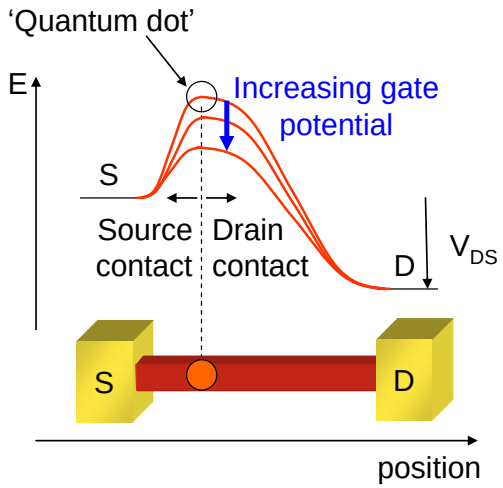



**Fig. 5.19.** An example of a typical potential profile along the length of a quantum wire as reflected by the bottom of the conduction band. The point of maximum potential acts as a barrier to the flow of current. As the gate bias increases, the barrier decreases, enhancing current flow. The point of maximum potential is modeled as a quantum dot with the same density of states as the quantum wire. The remainder of the wire is considered to be part of the contacts.

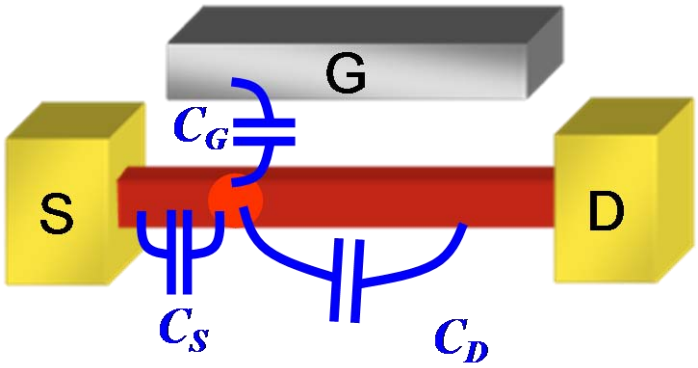



**Fig. 5.20.** Assuming the channel is modeled by a quantum dot we model the electrostatics of the transistor using capacitors.

**Ballistic Quantum Wire FET Current-Voltage Characteristics at T = 0K.**

The electrostatic capacitances are shown in Fig. 5.20 using the quantum dot model of the quantum wire. In this example we ignore source and drain capacitances. The gate capacitor was defined in Fig. 5.17 as $C_G$ = 1 aF per nanometer of gate length.

We compare quantum and electrostatic capacitances in Fig. 5.21, we find that the single mode wire has relatively few states, hence its quantum capacitance is small, and above the band edge it operates in the zero charging/insulator regime; even in the ON state charging effects are negligible and we can take $U = -qV_{GS}$.

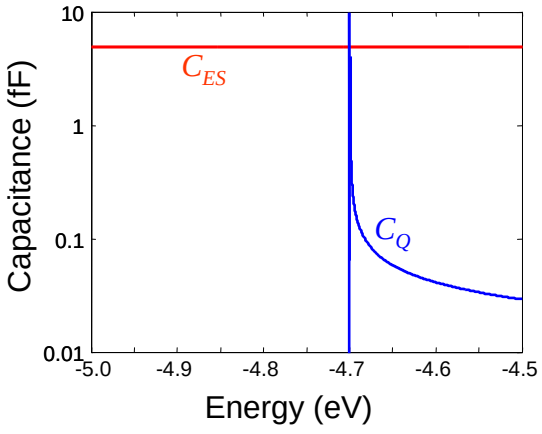



**Fig. 5.21.** A comparison between the electrostatic and quantum capacitances shows that that $C_Q >> C_{ES}$ only at the conduction band edge. But as the channel fills with charge, the wire returns to the insulator regime.

In forward bias (when the drain potential is lower than the source), there are three regimes of operation:

**(a) OFF: $V_{GS} < V_T$**

Let's define the threshold voltage as the potential difference between the source and the conduction band minimum. Thus, in this example, $V_T = 0.3$ V. Recall that the gate potential is relative to the source potential. So when $V_{GS} < V_T$, electrons cannot be injected from the source. Hence no current can flow for positive drain voltages. This is the OFF state of the FET.

Note that source drain current can flow for $T > 0$K since the tail of the Fermi distribution for electrons in the source overlaps with states in the wire. The current follows Eq. (5.25).

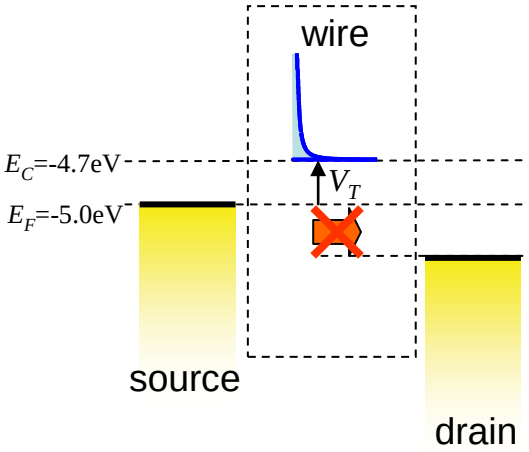



**Fig. 5.22.** Energy line up for FET in the OFF state. There are no channel states between the source and drain chemical potentials.

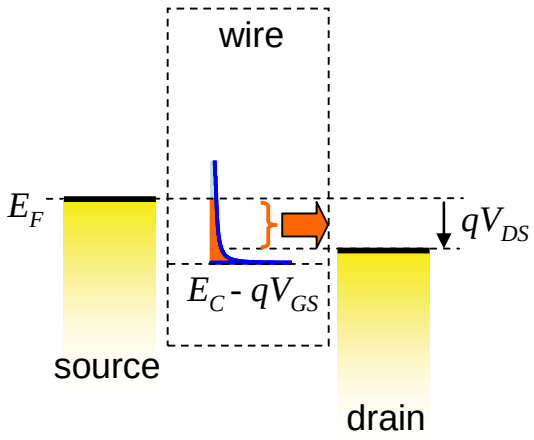
**(b) The linear regime: $V_{GS} > V_T$, $V_{DS} < V_{GS}$-$V_T$**

This is known as the linear regime because the current scales linearly with the drain source potential. Equation (5.43) reduces to

$$I_{DS} = \frac{2q^2}{h} V_{DS} \tag{5.44}$$

Note that the FET exhibits the quantum limit of conduction in this regime. Its transconductance, however, is zero.

**Fig. 5.23.** In the linear regime, the current is limited by the source drain potential.



**(c) Saturation: $V_{GS} > V_T$, $V_{DS} > V_{GS}-V_T$**

Once the drain potential exceeds $V_{GS}$-$V_T$, all the charge in the channel is uncompensated and injected into the drain. Thus, the current is limited by the gate potential. This is known as saturation.

$$I_{DS} = \frac{2q^2}{h}(V_{GS} - V_T) \tag{5.45}$$

The transconductance for a single mode wire in saturation is

$$g_m = \frac{2q^2}{h} \tag{5.46}$$

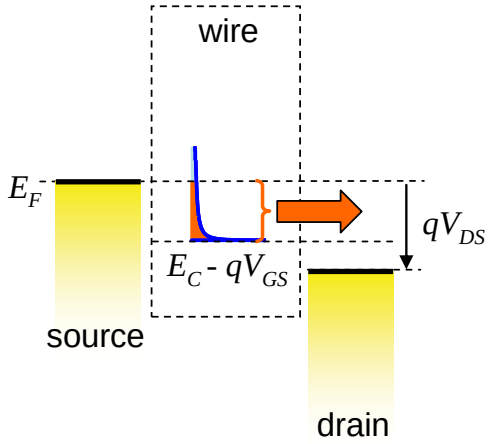



**Fig. 5.24.** In the saturation regime, the current is limited by the gate source potential.

Fig. 5.25 plots the forward bias characteristics of the FET both at T = 0K, and room temperature. At room temperature, the characteristics were determined numerically since the transition from linear to saturation regimes is blurred by thermal activation of electrons above the Fermi level.

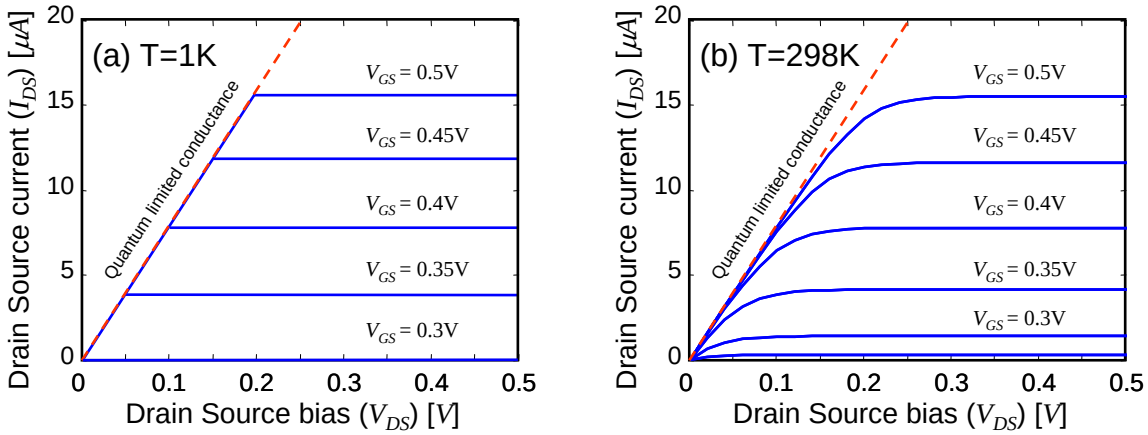



**Fig. 5.25.** Forward bias characteristics for a quantum wire FET at **(a)** T = 0K, and **(b)** room temperature.

## Part 5. Field Effect Transistors

### Ballistic Quantum Well FETs

To analyze the ballistic quantum well FET, let's begin with the master equation for current.

$$I = \frac{q\left(N_S - N_D\right)}{\tau} = \frac{q\left(N_S - N_D\right)v_x}{L} \tag{5.47}$$

We have defined conduction in the *x*-direction and the transit time is given by $\tau = L_x / v_x$ .

Let's begin by considering the product $g.v_x$, which we will integrate to get $(N_S - N_D)v_x$. In *k*-space and circular coordinates, this is

$$g\left(k\right)v_x\left(k\right)kdkd\theta = 2\frac{1}{\left(2\pi\right)^2/LW}\frac{\hbar k_x}{m}kdkd\theta \tag{5.48}$$

Simplifying further gives:

$$g\left(k\right)v_x\left(k\right)kdkd\theta = \frac{LW}{2\pi^2}\frac{\hbar}{m}k^2dk\sin\theta d\theta \tag{5.49}$$

Converting the variable of integration back to energy using the dispersion relation $E = \hbar^2k^2/2m + E_C + U$ , and assuming conduction in just a single mode of the quantum well, yields

$$g\left(k\right)v_x\left(k\right)kdkd\theta = \frac{LW}{2\pi^2\hbar^2}\sqrt{2m\left(E - E_C - U\right)}u\left(E - E_C - U\right)dE\sin\theta d\theta \tag{5.50}$$

Substituting back into Eq. (5.47) and integrating over the +*k* hemisphere ($0 < \theta < \pi$) gives

$$I = \frac{qW}{\pi^2\hbar^2}\int_{-\infty}^{\infty}\sqrt{2m\left(E - E_C - U\right)}u\left(E - E_C - U\right)\left(f\left(E,\mu_S\right) - f\left(E,\mu_D\right)\right)dE \tag{5.51}$$

Below threshold the density of states is zero. Thus,

$$U = -q\eta^0V_{GS} \tag{5.52}$$

where we neglect the effect of $V_{DS}$, and

$$\eta^0 = \frac{C_G}{C_S + C_D + C_G}\,. \tag{5.53}$$

The threshold voltage, $V_T$, is defined as the gate-source voltage required to turn the transistor ON, *i.e.* bring the bottom of the conduction band, $E_C$, down to the source workfunction. From Eq. (5.52) and requiring the $E_C + U = \mu_S$ at threshold, we get

$$V_T = \left(E_C - \mu_S\right)/\eta^0q \tag{5.54}$$

Above threshold the density of states and hence the quantum capacitance is constant. Thus, the quantum well FET is the rare case where we can model charging phenomena *analytically*. Above threshold we have

$$U = -\eta q\left(V_{GS} - V_T\right) - \eta^0qV_T \tag{5.55}$$

where again we neglect the effect of $V_{DS}$, and

$$\eta = \frac{C_G}{C_S + C_D + C_G + C_Q}\,. \tag{5.56}$$

Fom the 2-d DOS in Eq. (2.47), $C_Q$ for a single mode quantum well is

$$C_Q = \frac{1}{2} q^2 \frac{mWL}{\pi\hbar^2}. \tag{5.57}$$

where we have only considered half the usual density of states (the $+k$ states). This is accurate in the saturation region because the drain cannot fill any states in the channel. The quantum capacitance increases in the linear region as the drain fills some $-k$ states leading to errors in the calculation of the current in the linear regime.

Noting that $V_T = E_C / \eta^0 q$ we can rewrite Eq. (5.55) above threshold as

$$E_C + U = \mu_S - \eta q\left(V_{GS} - V_T\right). \tag{5.58}$$

Now, we can simplify Eq. (5.51) to give us

$$I = \frac{qW}{\pi^2\hbar^2} \int_{\mu_S - \eta q(V_{GS}-V_T)}^{\infty} \sqrt{2m\left(E + \eta q\left(V_{GS} - V_T\right)\right)}\left(f\left(E, \mu_S\right) - f\left(E, \mu_D\right)\right) dE \tag{5.59}$$

At $T$ = 0K, we can solve Eq. (5.59) in the linear regime ( $V_{DS} < \eta(V_{GS} - V_T)$ ):

$$\begin{aligned} I &= \frac{qW}{\pi^2\hbar^2} \int_{\mu_S - qV_{DS}}^{\mu_S} \sqrt{2m\left(E - E_C + \eta q V_{GS}\right)} dE \\ &= \frac{qW}{\pi^2\hbar^2} \sqrt{\frac{8m}{9}} (\eta q)^{3/2} \left[\left(V_{GS} - V_T\right)^{3/2} - \left(V_{GS} - V_T - V_{DS}/\eta\right)^{3/2}\right] \end{aligned} \tag{5.60}$$

and in the saturation regime ( $V_{DS} > \eta(V_{GS} - V_T)$ ):

$$\begin{aligned} I &= \frac{qW}{\pi^2\hbar^2} \int_{\mu_S - \eta q(V_{GS}-V_T)}^{\mu_S} \sqrt{2m\left(E + \eta q\left(V_{GS} - V_T\right)\right)} dE \\ &= \frac{qW}{\pi^2\hbar^2} \sqrt{\frac{8m}{9}} (\eta q)^{3/2} \left(V_{GS} - V_T\right)^{3/2} \end{aligned} . \tag{5.61}$$

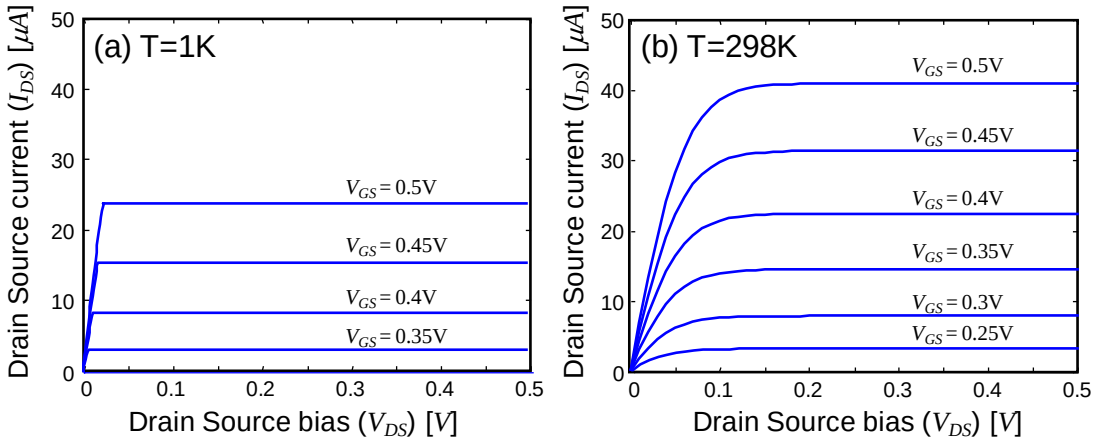



**Fig. 5.26.** Forward bias characteristics for a quantum well FET at **(a)** $T$ = 1K, and **(b)** room temperature. The channel width is $W$ = 120nm, and the electrostatic control over the channel is assumed to be ideal. Also, take $m = 0.5 \times m_0$.

Note that the saturation current goes as ~ $(V_{GS}\text{-}V_T)^{3/2}$ compared to the ballistic nanowire transistor, which goes as ~ $(V_{GS}\text{-}V_T)$. As we shall see, the conventional FET has a saturation current dependence of ~ $(V_{GS}\text{-}V_T)^2$.

### (iii) Conventional MOSFETs

Finally, we turn our attention to the backbone of digital electronics, the non-ballistic metal oxide semiconductor field effect transistor (MOSFET).

The channel material is a bulk *semiconductor* – typically silicon. Here, we will consider a so-called n-channel MOSFET, meaning that the channel current is carried by electrons at the bottom of the conduction band of the semiconductor.

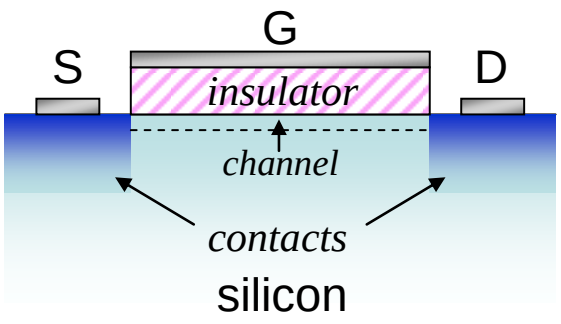



**Fig. 5.27.** An n-channel MOSET built on a silicon substrate. Phosphorous is diffused below the source and drain electrodes to form high conductivity contacts to the silicon channel beneath the insulator.

Now, let's consider the various operating regimes of a conventional MOSFET.

**(a) OFF: Subthreshold $V_{GS} < V_T$**

Similar to the ballistic quantum wire FET, we can model channel current as injection over a barrier close to the source electrode.

Once again, let's define the threshold voltage as the potential difference between the source Fermi energy and the conduction band minimum.[†]

As in the ballistic example, when $V_{GS} < V_T$, only the tail of the Fermi distribution for electrons in the source overlaps with empty states in the conduction band. The current follows Eq. (5.25).

$$I = I_0 \exp\left[\frac{qV_{GS}}{kT}\frac{C_G}{C_{ES}}\right] \tag{5.62}$$

Subthreshold characteristics determine the gate voltage required to switch the FET ON and OFF. From Eq. (5.27) the subthreshold slope is ideally 60mV/decade, meaning that a 60mV change in gate potential corresponds to a decade change in channel current.

[†] Actually, this is an overestimate of the threshold voltage because the density of states at the conduction band is so large that the transistor will often turn on when the Fermi level gets within a few *kT*. It also ignores the effect of charge trapped at the interface between the channel and the insulator.

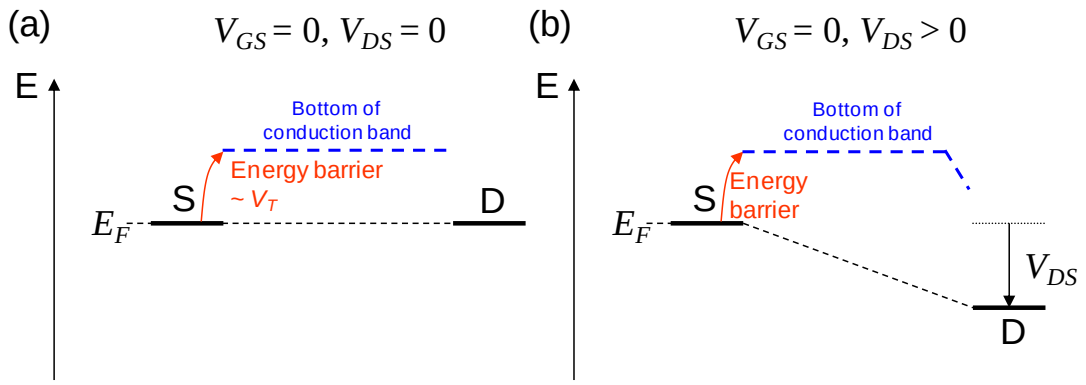



**Fig. 5.28.** Below threshold few electrons can be injected from the source into the conduction band, irrespective of the drain source potential.

**(b) The linear regime: $V_{GS} > V_T$, $V_{DS} < V_{GS}-V_T$**

As we shall see, this is known as the linear regime because the current scales linearly with the drain source potential. Consider a thin slice of the channel with width $W$, and length $\delta x$. For this analysis to hold, the length of this slice cannot be much shorter than the mean free path of the electron between scattering events. In a silicon transistor, we have shown that $\delta x >$ 50 nm (see the analysis associated with Fig. 4.23). Silicon transistors with channel lengths shorter than this should be analyzed in the ballistic regime.

Since the density of states above the conduction band is very large in a bulk semiconductor, a conventional MOSFET will enter the strong charging/metallic limit for $(V_{GS} - V) > V_T$, *i.e.* the number of charges, $\delta N$, in the slice is

$$q\delta N = \frac{C_G}{A} W \delta x \left(V_{GS} - V - V_T\right) \tag{5.63}$$

where $A = W.L$ is the surface area of the channel.

Now the current within the slice is given by

$$I = \frac{q\delta N}{\tau} \tag{5.64}$$

where $\tau$ is the lifetime of carriers within the channel slice.

Since scattering is important, we employ the classical model of charge transport to relate the charge carrier lifetime to velocity, $v$, and the length of the slice, $\delta x$.

$$I = q\delta N \frac{v}{\delta x} \tag{5.65}$$

Next we relate the charge carrier velocity to mobility

$$I = q\delta N \frac{\mu F}{\delta x} \tag{5.66}$$

Now, we must note that scattering causes the potential in the channel to vary with position. We define the channel potential $V(x)$ as a function of position in the channel. Thus, expressing the source-drain electric field in terms of the channel potential we have

$$I = q\frac{\mu}{\delta x}\delta N\frac{\delta V}{\delta x} \tag{5.67}$$

Next, we substitute Eq. (5.63) into Eq. (5.67), yielding

$$I = \mu\frac{C_G}{L}\left(V_{GS} - V - V_T\right)\frac{\delta V}{\delta x} \tag{5.68}$$

We solve this under the limit that $\delta x << L$, by integrating both sides with respect to $x$. Since the current is uniform throughout the channel, we obtain:

$$I.L = \int_0^L \mu\frac{C_G}{L}\left(V_{GS} - V - V_T\right)\frac{dV}{dx}dx \tag{5.69}$$

where $L$ is the length of the channel. It is convenient to change the variable of integration on the righthand side to voltage. In the linear regime, the maximum channel potential is $V_{DS}$, hence:

$$I = \mu\frac{C_G}{L^2}\int_0^{V_{DS}}\left(V_{GS} - V - V_T\right)dV \tag{5.70}$$

The linear regime requires that the entire channel remains in the strong charging/metallic limit. This occurs if the gate to drain potential, $V_{GD}$, also exceeds $V_T$

$$V_{GD} > V_T \tag{5.71}$$

or we can re-write this as

$$V_{DS} < V_{GS} - V_T \tag{5.72}$$

Under this constraint, Eq. (5.70) yields

$$I = \mu\frac{C_G}{L^2}\left(\left(V_{GS} - V_T\right)V_{DS} - \frac{1}{2}{V_{DS}}^2\right) \tag{5.73}$$

It is standard to express this in terms of a gate capacitance *per unit channel area*, $C_{OX}$:

$$I = \mu\frac{W}{L}C_{OX}\left(\left(V_{GS} - V_T\right)V_{DS} - \frac{1}{2}{V_{DS}}^2\right) \tag{5.74}$$

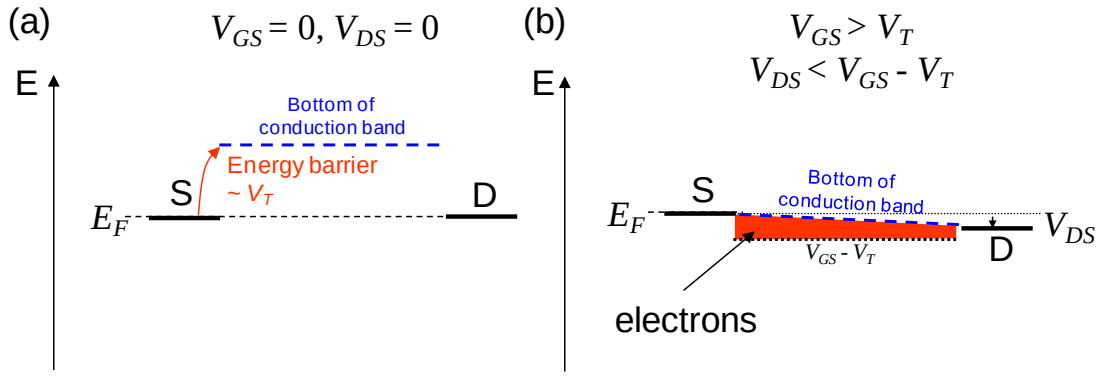



**Fig. 5.29.** Application of a gate source potential reduces the injection barrier between the source and the channel. The red shaded region represents the population of electrons in the conduction band. It does not represent filled states below the bottom of the conduction band.

**(c) Saturation: $V_{GS} > V_T$, $V_{DS} > V_{GS}$-$V_T$**

If the gate to drain potential exceeds threshold then the channel region close to the drain enters the zero charging regime, characterized by a high electric field and low density of mobile charges. The channel is said to pinch off and the current saturates because it is no longer dependent on $V_{DS}$. The strong charging/metallic region ends when the local channel potential $V = V_{GS} - V_T$

$$I = \int_0^{V_{GS}-V_T} \mu \frac{W}{L} C_{OX} \left(V_{GS} - V - V_T\right) dV \tag{5.75}$$

which gives

$$I = \mu \frac{W}{L} \frac{C_{OX}}{2} \left(V_{GS} - V_T\right)^2 \tag{5.76}$$

The *IV* characteristics of a non-ballistic MOSFET are shown in Fig. 5.31.

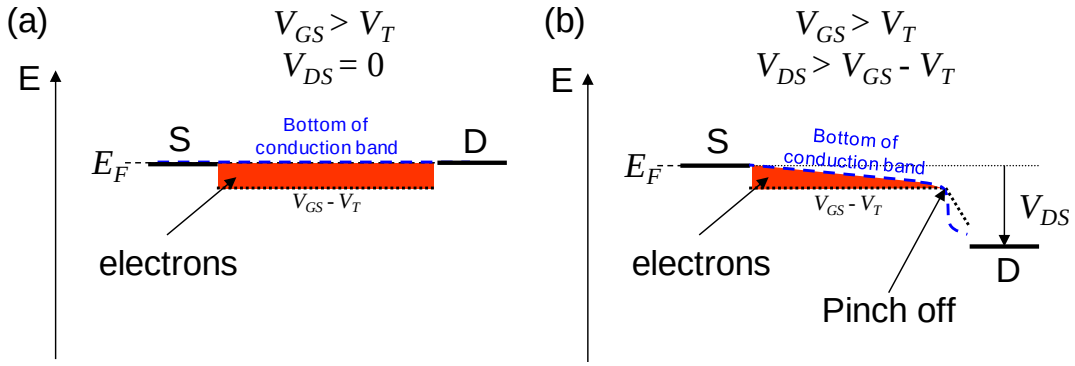



**Fig. 5.30.** As the drain-source potential increases, the channel near the drain enters the zero charging regime. The current is dependent only on the charge in the strong charging region, not on $V_{DS}$. The red shaded region represents the population of electrons in the conduction band. It does not represent filled states below the bottom of the conduction band.

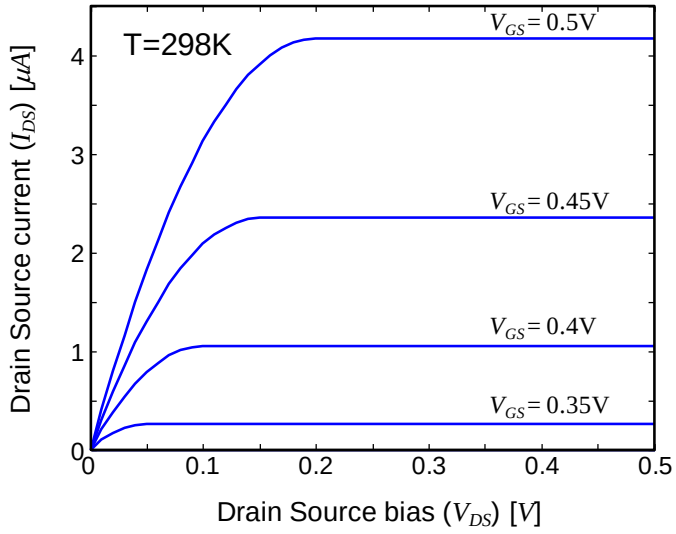



**Fig. 5.31.** The IV characteristics of a non-ballistic MOSFET with $\mu$ = 300 cm$^2$/Vs, $L$ = 40nm, $W = 3 \times L$, $V_T$ = 0.3V, and $C_G$ = 0.1 fF. Note that the use of the classical model for a transistor with such a short channel is inappropriate.

# Part 5. Field Effect Transistors

### Comparison of ballistic and non-ballistic MOSFETs.

If we calculate the *IV* of a conventional MOSFET with a channel length in the ballistic regime, we obtain *IV* curves that are qualitatively similar to the ballistic result. For example, the classical model of a MOSFET with a channel length of 40 nm is shown in Fig. 5.31. It is qualitatively similar to Fig. 5.26. Both possess a linear and a saturation regime, and both exhibit identical subthreshold behavior. But the magnitude of the current differs quite substantially. The ballistic device exhibits larger channel currents due to the absence of scattering.

Another way to compare ballistic and non-ballistic MOSFETs is to return to the water flow analogy.[†] As before, the source and drain are modeled by reservoirs. The channel potential is modeled by a plunger. Gate-induced changes in the channel potential cause the plunger to move up and down in the channel. The most important difference between the ballistic and non-ballistic MOSFETs is the profile of the water in the channel. The height of the water changes in the non-ballistic device, whereas water in the ballistic channel does not relax to lower energies during its passage across the channel.

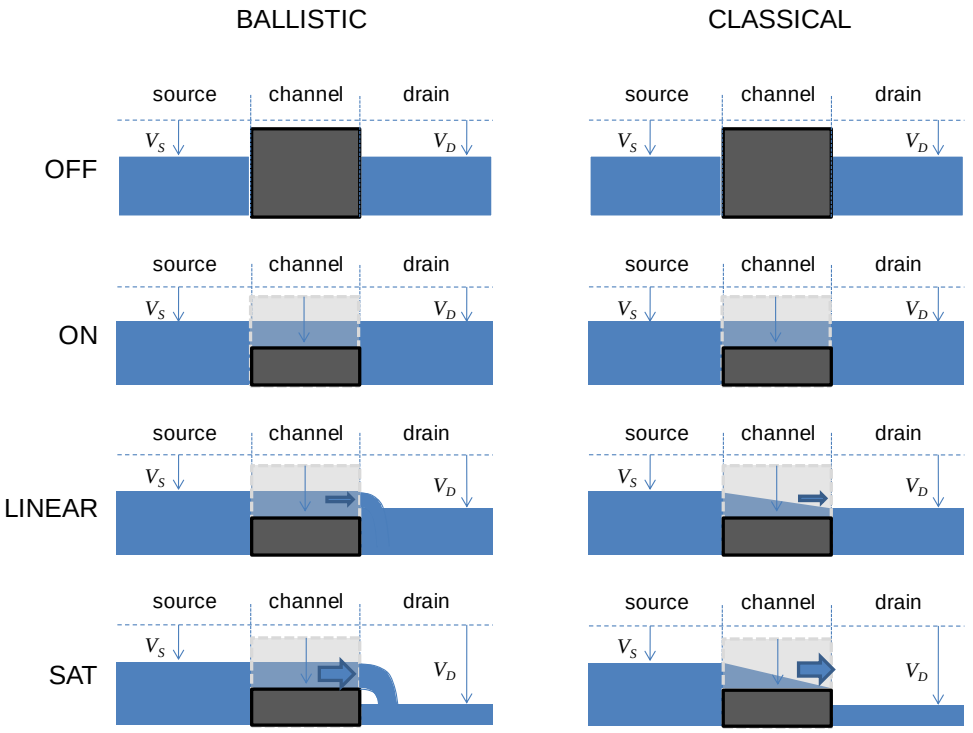



**Fig. 5.32.** The water flow analogy for the operation of ballistic and classical MOSFETs. Conduction in the channel is controlled by a plunger that models the channel potential. The transistors are turned ON by lowering the gate potential. Then, as the height of the drain reservoir decreases (corresponding to increased $V_{DS}$), the channel first enters the linear regime (where current flow is limited by $V_{DS}$) and then the saturation regime where the current is controlled only by the gate potential.

[†] For a more detailed treatment of the water analogy to conventional FETs see Tsividis, 'Operation and Modeling of the MOS transistor', 2nd edition, Oxford University Press (1999).

**Problems**

**1. Buckyball FETs**

Park *et al.* have reported measurements of a buckyball (C60) FET. An approximate model of their device is shown in Fig. 5.33. The measured conductance as a function of $V_{DS}$ and $V_{GS}$ is shown in Fig. 5.34.

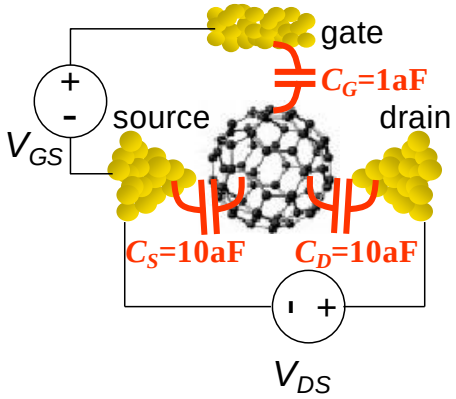



**Fig. 5.33.** The geometry of a C60 FET. In addition take the temperature to be T = 1K, and the molecular energy level broadening, Γ = 0.1eV. The LUMO is at -4.7 eV and the Fermi Energy at equilibrium is $E_F$ = -5.0 eV

**(a)** Calculate the conductance ($dI_{DS}/dV_{DS}$) using the parameters in Fig. 5.33. Consider $5V < V_{GS} < 8V$ calculated at intervals of 0.2V and $-0.2V < V_{DS} < 0.2V$ calculated at intervals of 10mV.

**(b)** Explain the X-shape of the conductance plot.

**(c)** Note that Park, *et al.* measure a non-zero conductance in the upper and lower quadrants. Sketch their $I_{DS}$-$V_{DS}$ characteristic at $V_{GS} \sim 5.9V$. Compare to your calculated $I_{DS}$-$V_{DS}$ characteristic at $V_{GS} \sim 5.9V$. Propose an explanation for the non-zero conductances measured in the experiment in the upper and lower quadrants.

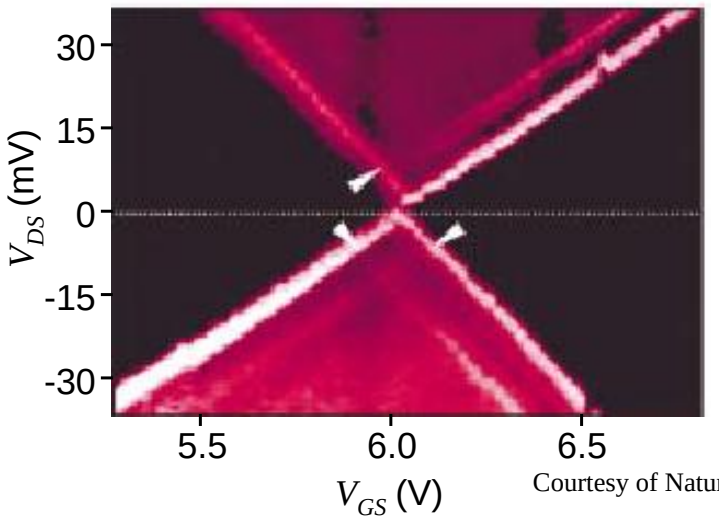



**Fig. 5.34.** The conductance ($dI_{DS}/dV_{DS}$) of a C60 FET as measured by Park *et al.* Ignore the three arrows on the plot. From Park, *et al.* "Nanomechanical oscillations in a single C60 transistor" Nature **407** 57 (2000).

**(d)** In Park *et al.*'s measurement the conductance gap vanishes at $V_{GS}$ = 6.0V. Assuming that $C_G$ is incorrect in Fig. 5.33, calculate the correct value.

**Reference**

Park, *et al.* "Nanomechanical oscillations in a single C60 transistor" Nature **407** 57 (2000)

**2. Two mode Quantum Wire FET**

Consider the Quantum Wire FET of Fig. 5.17 in the text.

Assume that the quantum wire has <u>two</u> modes at $E_{C1}$ = -4.7eV, and $E_{C2}$ = -4.6eV. Analytically determine the $I_{DS}$-$V_{DS}$ characteristics for varying $V_{GS}$ at $T$ = 0K. Sketch your solution for 0 < $V_{DS}$ < 0.5, at $V_{GS}$ = 0.3 V, 0.35 V, 0.4V, 0.45V and 0.5V.

Highlight the difference in the IV characteristics due to the additional mode.

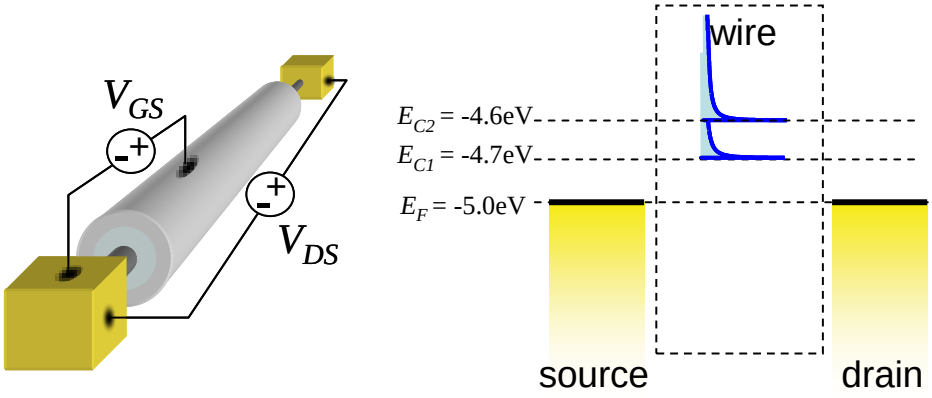



**Fig. 5.35.** A quantum wire FET with two modes. The length of the wire is $L$ = 100nm, the gate capacitance is $C_G$ = 50 aF <u>per nanometer of wire length</u>, and the electron mass, $m$, in the wire is $m = m_0$=9.1x10$^{-31}$ kg. Assume $C_S$ and $C_D$ = 0.

**3. 2-d ballistic FET**

**(a)** Numerically calculate the current-voltage characteristics of a single mode 2-d ballistic FET using Eq. (5.51) and a self consistent solution for the potential, $U$. Plot your solution for $T$ = 1K and $T$ = 298K. In each plot, consider the voltage range 0 < $V_{DS}$ < 0.5, at $V_{GS}$ = 0.3 V, 0.35 V, 0.4V, 0.45V and 0.5V. In your calculation take the bottom of the conduction band to be -4.7 eV, the Fermi Energy at equilibrium $E_F$ = -5.0 eV, $L$ = 40nm, $W = 3 \times L$, and $C_G$ = 0.1 fF. Assume $C_D = C_S = 0$. Take the effective mass, $m$, as $m = 0.5 \times m_0$, where $m_0$ = 9.1x10$^{-31}$ kg.

You should obtain the IV characteristics shown in Fig. 5.26.

*Continued on next page….*

**(b)** Next, compare your numerical solutions to the analytic solution for the linear and saturation regions (Eqns (5.60) and (5.61)). Explain the discrepancies.

**(c)** Numerically determine $I_{DS}$ vs $V_{GS}$ at $V_{DS}$ = 0.5V and $T$ = 298K. Plot the current on a logarithmic scale to demonstrate that the transconductance is 60mV/decade in the subthreshold region.

**(d)** Using your plot in (c), choose a new $V_T$ such that the analytic solution for the saturation region (Eq. (5.61)) provides a better fit at room temperature. Explain your choice.

**4.** An experiment is performed on the channel conductor in a three terminal device. Both the source and drain are grounded, while the gate potential is varied. Assume that $C_G >> C_S, C_D$.

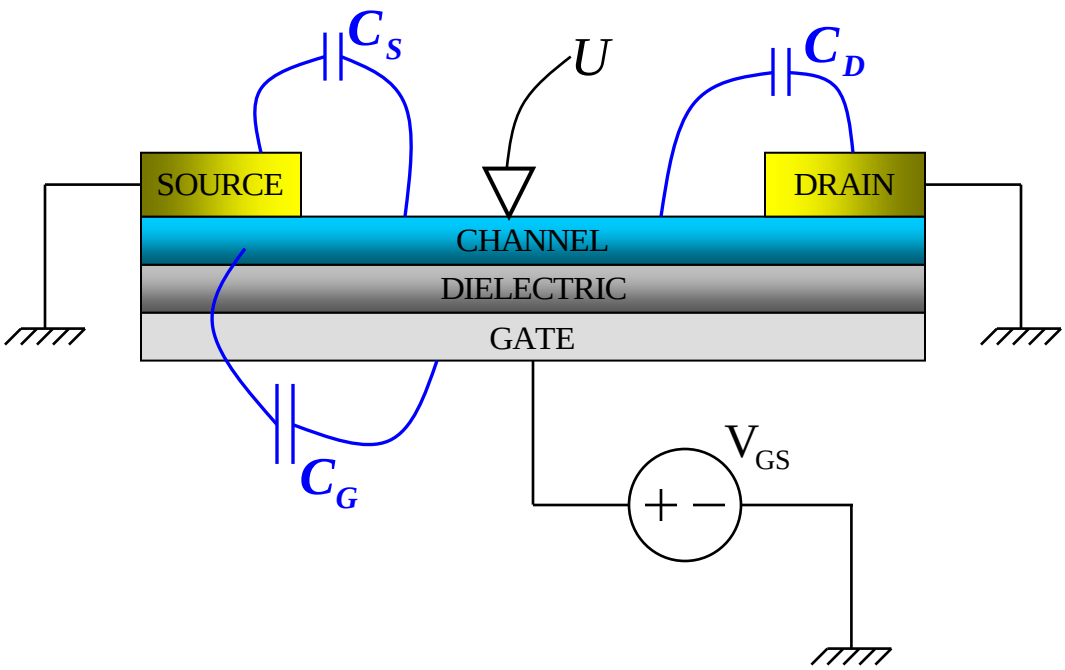



**Fig. 5.36.** Measuring the surface potential of a transistor channel.

The transistor is biased above threshold ($V_{GS} > V_T$). Measurement of the channel potential, $U$, shows a linear variation with increasing $V_{GS} > V_T$.

Under what conditions could the conductor be:

(i) a quantum dot (0 dimensions)?
(ii) a quantum wire (1 dimension)?
(iii) a quantum well (2 dimensions)?

Explain your answers.

## Part 5. Field Effect Transistors

**5.** Consider a three terminal molecular transistor.

**(a)** Assume the molecule contains only a single, unfilled molecular orbital at energy $\Delta$ above the equilibrium Fermi level. Assume also that $C_G >> C_S$, $C_D$ and $\Delta >> kT$. Calculate the transconductance for small $V_{DS}$ as a function of $T$ and $V_{GS}$ for $V_{GS} << \Delta$.

Express your answer in terms of $I_{DS}$.

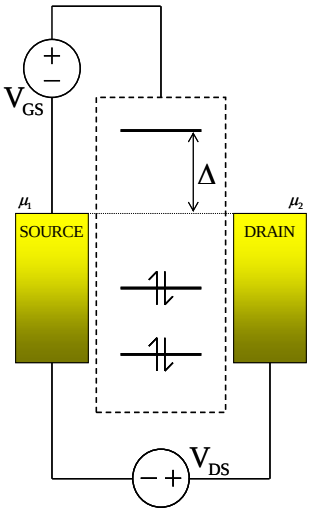



**Fig. 5.37.** A molecular transistor with discrete energy levels in the channel.

**(b)** Now, assume that the density of molecular states is

$$g(E) = \frac{1}{E_T} \exp\left[\frac{E-\Delta}{E_T}\right] u(\Delta - E)$$

where $E_T >> kT$. Calculate the transconductance for small $V_{DS}$ as a function of $T$ and $V_{GS}$ for $V_{GS} << \Delta$. Assume $C_G \to \infty$.

Express your answer in terms of $I_{DS}$.

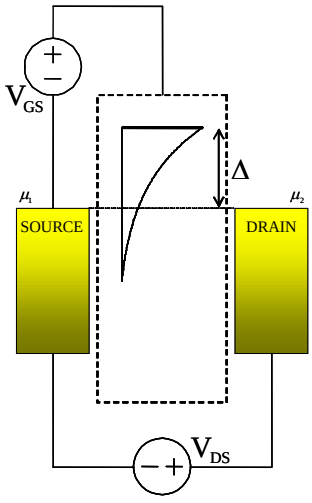



**Fig. 5.38.** A molecular transistor with an exponential DOS in the channel.

**(c)** Discuss the implications of your result for molecular transistors.

**6.** Consider the conventional n-channel MOSFET illustrated below:

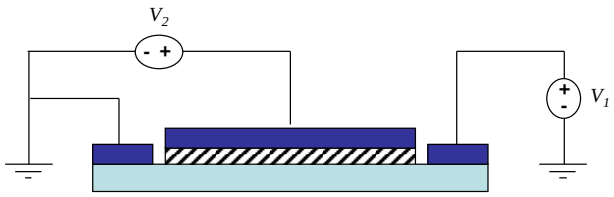



**Fig. 5.39.** The structure of a conventional MOSFET.

Assume $V_T$ = 1V and $V_2$ = 0V. Sketch the expected *IV* characteristics ($I$ vs. $V_1$) and explain, with reference to band diagrams, why the *IV* characteristics are not symmetric.

**7.** Consider a ballistic quantum well FET at $T$ = 0K.

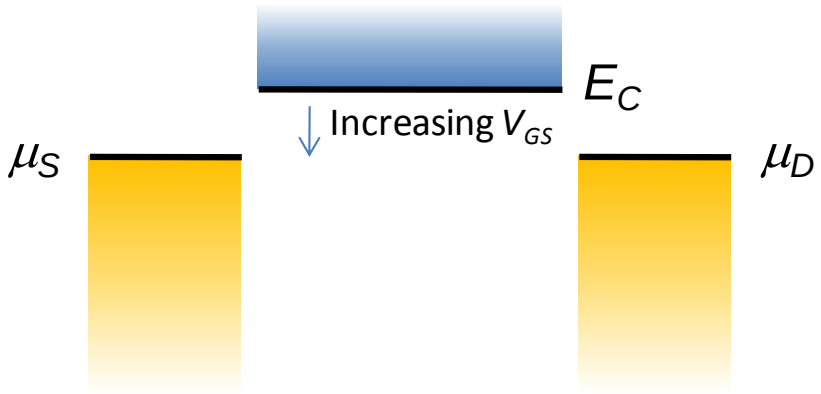



**Fig. 5.40.** A quantum well FET below threshold.

Recall that the general solution for a quantum well FET in saturation is:

$$I_{DS} = \frac{qW}{\pi^2\hbar^2}\sqrt{\frac{8m}{9}}\left(\eta q\left(V_{GS}-V_T\right)\right)^{3/2}$$

**(a)** In the limit that $C_Q >> C_{ES}$, the bottom of the conduction band, $E_C$, is 'pinned' to $\mu_S$ at threshold. Show that under these conditions $\eta \rightarrow 0$.

**(b)** Why isn't the conductance of the channel zero at threshold in this limit?

**(c)** Given that $C_{OX} = C_G/(WL)$, where $W$ and $L$ are the width and length of the channel, respectively, show that the saturation current in this ballistic quantum well FET is given by

$$I_{DS} = \frac{8\hbar W}{3m\sqrt{\pi q}}\left(C_{OX}\left(V_{GS}-V_T\right)\right)^{3/2} \qquad (5.77)$$

Hint: Express the quantum capacitance in the general solution in terms of the device parameters $m$, $W$, and $L$.

## Part 5. Field Effect Transistors

**8.** A quantum well is connected to source and drain contacts. Assume identical source and drain contacts.

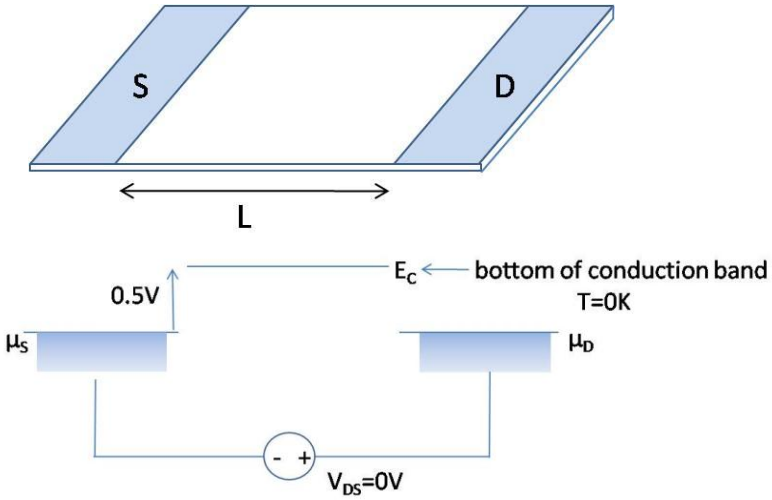



**Fig. 5.41.** A quantum well with source and drain contacts.

**(a)** Plot the potential profile along the well when $V_{DS}$ = +0.3V.

Now a gate electrode is positioned above the well. Assume that $C_G \gg C_S, C_D$, except very close to the source and drain electrodes. At the gate electrode $\varepsilon = 4\times8.84\times10^{-12}$ *F/m* and $d = 10nm$. Assume the source and drain contacts are identical.

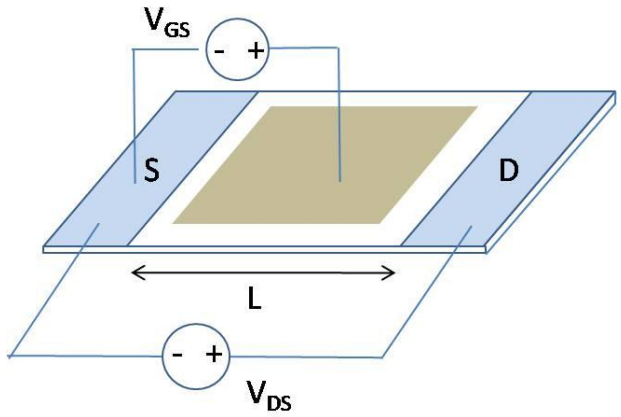



**Fig. 5.42.** The quantum well with a gate electrode also.

**(b)** What is the potential profile when $V_{DS}$ = 0.3V and $V_{GS}$ = 0V.

**(c)** Repeat (b) for $V_{DS}$ = 0V and $V_{GS}$ = 0.7V. Hint: Check the $C_Q$.

**(d)** Repeat (b) for $V_{DS}$ = 0.3V and $V_{GS}$ = 0.7V assuming ballistic transport.

**(e)** Repeat (b) for $V_{DS}$ = 0.3V and $V_{GS}$ = 0.7V assuming non-ballistic transport.

**9.** This problem considers a 2-d quantum well FET. Assume the following:

$T$ = 0K, $L$ = 40nm, $W$ = 120nm, $C_G$ = 0.1fF , $C_S = C_D = 0$

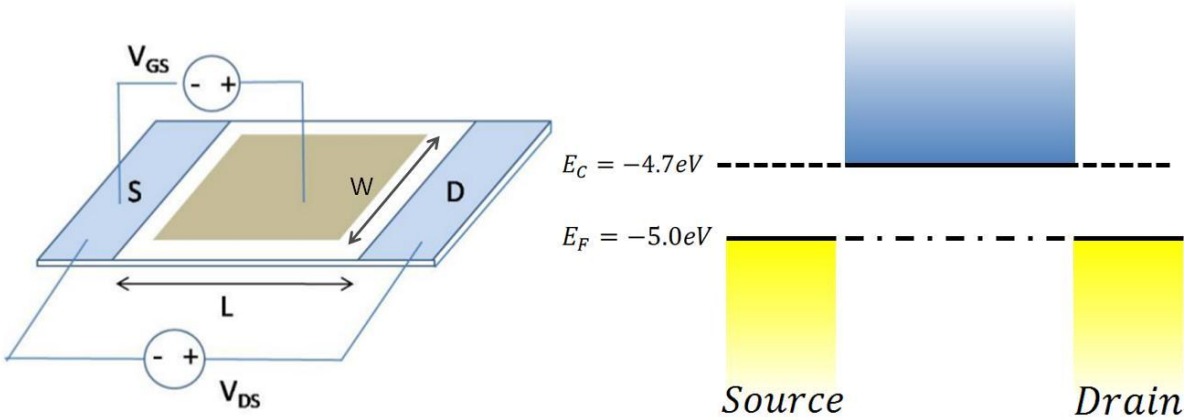



**Fig. 5.43.** A 2-d quantum well FET.

**(a)** Compare the operation of the 2-D well in the ballistic and semi-classical regimes. **Assume $C_Q \to \infty$ >> $C_{ES}$ in both regimes.**
Take $\mu$ = 300 cm$^2$/Vs in the semi-classical regime.

Plot $I_{DS}$ vs $V_{DS}$ for $V_{GS}$ = 0.5V and $V_{DS}$ = 0 to 0.5V.

(**b)** Explain the difference in the IV curves. Is there a problem with the theory? If so, what?

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