Code No: 5455AP 178R105509 **R17**

**JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD**
**M. Tech II Semester Examinations, June/July - 2018**
**SYSTEM ON CHIP ARCHITECTURE**
**(Embedded Systems)**

**Time: 3hrs** **Max.Marks:75**

**Note:** This question paper contains two parts A and B.
Part A is compulsory which carries 25 marks. Answer all questions in Part A. Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 10 marks and may have a, b, c as sub questions.

**PART - A**

**5 × 5 Marks = 25**

1.a) Mention about the system level interconnections and their applications. [5]
b) Distinguish between the more robust processors and vector processors. [5]
c) Mention the different Write Policies used in memory design for SOC. [5]
d) Discuss the effects of bus transactions and contention time [5]
e) Write about the Design and evaluation procedures. [5]

**PART - B**

**5 × 10 Marks = 50**

2. Discuss about system architectures and the different components of the system. [10]

**OR**

3. Write about the SOC memory and addressing requirements and discuss about the operating system needs for SOC [10]

4.a) Discuss the process of minimizing pipeline delays in SOC.
b) Briefly explain about the instruction decoders and interlocks. [5+5]

**OR**

5. Explain the basic concepts in processor micro architecture and discuss about the vector processors. [10]

6. Discuss the SOC external memory and internal memory and mention the models of simple processor – memory interaction. [10]

**OR**

7. Describe the different types of Caches and differentiate split-I, D–cache, multilevel Caches. [10]

8. Discuss the SOC Standard Buses and write about the bus models with their components in brief. [10]

**OR**

9. Discuss about the Instance Specific design in SOC and write about the Customizable Soft Processor and its requirements. [10]

10. Describe the approaches for designing SOC devices with their required specifications. [10]

**OR**

11. Explain about the quick MIPS block diagram for the AES SOC system. [10]

---oo0oo---