Code No: 5455AB

R17

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

M.Tech I Semester Examinations, January - 2018

ARM PROCESSOR ARCHITECTURES

(Embedded Systems)

Time: 3hrs **Max.Marks:75**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 25 marks. Answer all questions in Part A. Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 10 marks and may have a, b, c as sub questions.

PART - A

5 × 5 Marks = 25

1.a) Explain how a constant is loaded into a general purpose register of ARM processor. [5]

b) The interrupt service is quite powerful in ARM. Explain the need for a fast interrupt service and a normal interrupt service with their own stack operations. [5]

c) Explain the while loop control structure with simple example. [5]

d) Write a short on paging memory management scheme. [5]

e) Explain the concept of integer normalization. [5]

PART - B

5 × 10 Marks = 50

2. What is current program status register? Explain the generic structure of program status register as ARM core. [10]

OR

3. Explain different data processing instructions in ARM (with examples). [10]

4. Define Exception and explain how to handle Exception in ARM. [10]

OR

5. List the most notable features of the ARM Thumb instruction set. [10]

6. Write a program using C language to print "Hello World" on display before terminating. [10]

OR

7. Write short note on following.
a) Functions b) Procedures [5+5]

8. Draw separate instruction and data cache (Modified Harvard architecture) and explain the operation of it. [10]

OR

9. Explain how memory is organized in ARM processor. [10]

10. Write assembly program for signed 64 bit by 64 bit multiply with 128 bit result and explain about it. [10]

OR

11. Explain about random number generation methods for ARM processor. [10]

---oo0oo---