Code No: 5255AP

R15

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
M. Tech II Semester Examinations, August - 2016
DIGITAL SIGNAL PROCESSORS AND ARCHITECTURES
(Embedded Systems)

Time: 3hrs

Max.Marks:75

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 25 marks. Answer all questions in Part A. Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 10 marks and may have a, b, c as sub questions.

PART - A

5 × 5 Marks = 25

1.a) What is pipelining? Discuss with examples. [5]
b) Explain the memory space of TMS320C54XX processors. [5]
c) What are programmer's model states? [5]
d) Describe briefly the assembly language syntax. [5]
e) What is MVFR1? [5]

PART – B

5 × 10 Marks = 50

2.a) Describe discrete Fourier transform (DFT) and Fast Fourier transform (FFT).
b) Assuming X(k) as a complex sequence, determine the number of complex and real multiplies for computing IDFT using direct and radix – 2 FFT algorithms.
c) The signal sequence x(n) = {0 2 4 6 8} is interpolated using the interpolation filter sequence b_k = [0.5 1 0.5] and the interpolation factor is 2. Determine the interpolated sequence y(m). [3+3+4]

OR

3.a) Explain system level pipelining.
b) What is the bit – reversed sequence of 32 samples $x_0, x_1, x_2, \ldots\ldots, x_{31}$ as obtained by sampling a signal?
c) What architectural features are required in a DSP device to implement an FIR filter with N taps so that a steady – state through put of one output sample per cycle is achieved? [3+3+4]

4.a) Explain the pipeline operation of TMS320C54XX processors.
b) Write a TMS320C54XX program to implement second-order IIR filter equations
$d(n) = x(n) + d(n-1)\, a_1 + d(n-2)\, a_2$
$y(n) = d(n)\, b_0 + d(n-1)\, b_1 + d(n-2)\, b_2$
where a_1, a_2, b_0, b_1, b_2 are filter coefficients (integers), x(n) is the latest input sample, y(n) is the filtered output sample, and d(n) is an intermediate result. You may assume that, during calculations, all signals remain within values represented by 16 bits.
c) Write a TMS320C54XX program to read 100h words from the input port at address INPORT and store them in the data memory starting at address BUFFER. [3+4+3]

OR

5.a) Explain the function of on – chip peripherals.

b) What is the role of the interrupt pins in a DSP device? Are these the only means of interrupting a DSP program? How do you prevent a signal on an interrupt pin from interrupting a time – critical program being executed by the DSP?

c) By means of a figure, explain the pipeline operation of the following sequence of TMS320C54XX instructions if the initial value of AR3 is 80 and the values stored in memory location 80, 81, 82 are 1, 2, and 3. [3+3+4]

```
LD *AR3+, A
ADD *AR3+, A
STL A, *AR3+
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6.a) Explain system control block (SCB).

b) Describe the features of the cortex – M3 and cortex – M4 processors. [5+5]

OR

7.a) Explain nested vectored interrupt controller (NVIC).

b) Describe scalability and compatibility of ARM processors. [5+5]

8.a) Describe cortex – M4 specific instructions.

b) What is barrel shifter? [5+5]

OR

9.a) How do you access special instructions in programming?

b) How do you access special registers in programming? [5+5]

10.a) Give FP registers review.

b) Describe CPACR register. [5+5]

OR

11.a) What is FPCAR?

b) What is FPDSCR? [5+5]

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