Code No: 57017 **R09**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

B. Tech IV Year I Semester Examinations, November - 2015

VLSI DESIGN

(Electrical and Electronics Engineering)

Time: 3 Hours **Max. Marks: 75**

Answer any Five Questions

All Questions Carry Equal Marks

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1.a) With neat sketches explain the formation of inversion layer in n-channel enhancement MOSFET.

b) What is the purpose of metallization in IC manufacturing? Explain the methods employed for metallization. [8+7]

2.a) Draw the circuit of nMOS inverter with depletion mode NMOS as a load and explain its operation and characteristics.

b) Explain the operation of BiCMOS inverter. Clearly specify its characteristics. [8+7]

3.a) Describe briefly the process of VLSI design flow.

b) Write the scaling factors for different types of scaling parameters. [8+7]

4.a) Enumerate the steps of designing complex boolean functions using CMOS logic.

b) Derive the expression for propagation delay in cascaded pass transistors. [8+7]

5.a) Design a magnitude comparator based on the datapath operators?

b) Explain synchronous and asynchronous counter structures. [7+8]

6.a) Draw and explain basic memory-chip architecture.

b) Explain in detail about CAM. [8+7]

7.a) Draw the schematic structure for PLA and explain its principle. What are the advantages of PLAs?

b) With neat schematic explain the architectural building blocks of CPLD. [8+7]

8.a) Explain the scan-path design technique used to test sequential circuit in detail.

b) Explain about BIST pertaining to VLSI testing. [8+7]

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