Code No: 54010 **R09**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY, HYDERABAD
B.Tech II Year II Semester Examinations, November/December - 2015
SWITCHING THEORY AND LOGIC DESIGN
(Common to EEE, ECE, BME, ETM)

Time: 3 hours **Max. Marks: 75**

Answer any five questions
All questions carry equal marks

1.a) Write a note on floating point representation of numbers and determine the number of bits required to represent in floating point notation the exponent for decimal numbers in the range of $10^{\pm 86}$.

b) Write the arithmetic rules for addition, subtraction, multiplication and division. Divide the following binary numbers
i) 11001 ÷ 101 ii) 11101 ÷ 1100 [7+8]

2.a) What are universal gates? Implement all the basic gates using universal gates and wtite the truth table for each gate.

b) Simplify Y = Σm(3,6,7,8,10,12,14,17,19,20,21,24,25,27,28) using K-map method. [7+8]

3.a) Find the minimal sum of products for the Boolean expression
f = Σm(1,2,3,7,8,9,10,11,14,15) using the tabular method.

b) If $\bar{A}B + C\bar{D} = 0$, then prove that $AB + \bar{C}(\bar{A} + \bar{D}) = AB + BD + \bar{B}\bar{D} + \bar{A}\bar{C}D$. [8+7]

4.a) With a neat logic diagram explain the operation for carry look ahead adder.

b) Write a short note on:
i) Encoder ii) Decoder iii) Mulitplexer iv) Demultiplexer. [7+8]

5.a) Tabulate the PLA programming table for the four Boolean functions listed below
A(x,y,z) = Σm(1,2,4,6)
B(x,y,z) = Σm(0,1,6,7)
C(x,y,z) = Σm(2,6)
D(x,y,z) = Σm(1,2,3,5,7)

b) A combinational circuit is defined by the functions F_1= Σm(3,5,7) and F_2=Σm(4,5,7), implement the circuit with a PLA having 3 inputs, 3 product terms and two outputs. [8+7]

6.a) Write the excitation table for SR flipflop. Design a synchronous MOD-6 Counter using SR-Flipflop for the following count sequence 0,1,3,2,6,4 and repeat. Write the transition table and logic diagram.

b) What is a sequential circuit? Discuss the different types of sequential circuits. [10+5]

7.a) Describe the steps involved in the minimization of completely specified sequential machines using partition techniques.

b) With a neat sketch explain about Moore model and Mealy model sequential networks. [8+7]

8.a) Design an overlapping sequence detector that detects a sequence of 101101 using ASM charts.

b) Explain in detail about the ASM technique of designing the sequential circuit. [8+7]

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