

Code No: 113BS

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

B.Tech II Year I Semester Examinations, November - 2015

DIGITAL LOGIC DESIGN

(Computer Science and Engineering)

Time: 3 Hours

Max. Marks: 75

Note: This question paper contains two parts A and B.

Part A is compulsory which carries 25 marks. Answer all questions in Part A.

Part B consists of 5 Units. Answer any one full question from each unit.

Each question carries 10 marks and may have a, b, c as sub questions.

PART-A

(25 Marks)

- 1.a) State and Prove De Morgan's Theorems. [2M]
- b) Realize an XOR gate using universal gates. [3M]
- c) Write about Sum of Products and Product of Sums of Boolean expressions. [2M]
- d) Explain Steps of Simplification in Karnaugh maps with example. [3M]
- e) Explain the working of Full adder with help of diagram. [2M]
- f) Draw the logic diagram of a 3/8 decoder. [3M]
- g) Construct Master-Slave J-K Flip-Flop. [2M]
- h) Explain about Ripple counter. [3M]
- i) Differentiate between SRAMs and DRAMs. [2M]
- j) What is the difference between PLA and PAL? [3M]

PART-B

(50 Marks)

- 2.a) Explain various number systems and Binary codes used in digital logic design with examples.
- b) Draw the logic diagram of the Boolean expression without simplifying $(A+B)(C+D)(\bar{A}+B+D)$. [5+5]

OR

- 3.a) Explain the signed binary number representation and floating point number representation with typical examples and discuss about their advantages.
- b) Convert $(AB+C)(B+\bar{C}D)$ expression into sum of products and product of sums form. [5+5]

- 4.a) Realize the following function using basic gates. (Two-level).

$$f(x, y, z) = \sum(3, 5, 6, 7)$$

- b) Simplify the Boolean function F together with don't care condition d , and then express the simplified function in some of minterms: $F(A, B, C, D) = \sum(0, 2, 5, 7, 11, 15), d = \sum(3, 4, 6, 12, 13)$. [5+5]

OR

- 5.a) Construct Karnaugh maps for three variable, four variable and five variable Boolean functions and discuss their simplification methods.
- b) Implement the following Boolean function using NAND gates and NOR gates after simplification using Karnaugh map method: $F(A, B, C) = \sum(0, 1, 2, 3, 6, 7)$. [5+5]

- 6.a) Discuss with example how higher order Decoders are realized using low-order Decoders.
- b) Draw the logic diagrams of a 4 bit binary to gray and gray to binary code converter and verify its working with suitable examples. [5+5]

OR

- 7.a) Explain the functions of a De multiplexer and Encoder with necessary diagrams and discuss their applications.
- b) Construct logic diagram of a 4bit 2's complement adder for performing subtraction operation and verify its working by taking suitable examples. [5+5]

- 8.a) Draw the circuit diagram of a 4 bit UP/DOWN binary counter and explain its working with the help of its state diagram and truth table.
- b) Design a 4 bit binary Ripple counter using T flip-flops and explain its working with help of state diagrams and truth table. [5+5]

OR

- 9.a) Design a 4 bit universal shift register and explain its working with the help of its state diagram and timing diagram.
- b) Explain the working of synchronous sequential circuits and asynchronous sequential circuits with examples and mention their applications. [5+5]

- 10.a) Explain various types of memories and their construction and characteristics and discuss the hierarchy of memory organization.

- b) Implement the following two Boolean functions with a PLA

$$F_1(A, B, C) = \sum (0, 2, 4, 6)$$

$$F_2(A, B, C) = \sum (0, 1, 6, 7)$$

[5+5]

OR

- 11.a) What is Cache memory? Explain the organization of cache memory with suitable diagrams.
- b) What is meant by memory decoding? Discuss the structure of address bus and data bus with suitable diagrams. [5+5]

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