Code No: 53024 **R09**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

B.Tech II Year I Semester Examinations, November - 2015

DIGITAL LOGIC DESIGN

(Computer Science and Engineering)

Time: 3 hours **Max. Marks: 75**

Answer any five questions

All questions carry equal marks

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1.a) Explain the base conversions for binary numbers, octal numbers and hexadecimal numbers for the given decimal numbers: i) 345 ii) 625 iii) 26.625.

b) Explain Binary codes, ASCII codes, Excess-3 codes, Gray codes, Error detecting codes and Error correcting codes with examples for each code. [7+8]

2.a) Describe the basic theorems and properties of Boolean algebra.

b) State and prove De Morgan theorems and verify the theorems using Logic gates.

c) Express the following function in sum of minterms and product of maxterms.
$F(A,B,C,D) = B'D + A'D + BD$. [5+5+5]

3.a) Explain the methods of simplification of Boolean expression using Karnaugh methods by taking 4 variable function that includes Don't care conditions.

b) Simplify the following four variable Boolean function and implement the same using NAND logic. $F(A, B, C, D) = \sum (0, 2, 4, 5, 6, 7, 8, 10, 13, 15)$. [7+8]

4.a) Discuss the analysis and design procedure and draw the logic diagram of a 4 bit BCD adder.

b) Write an HDL gate level description and HDL behavioral description of a BCD - to- excess-3 code converter. [7+8]

5.a) Explain the differences among a truth table, a state table, a characteristic table and an excitation table by taking suitable example.

b) A sequential circuit has two JK flip-flops A and B and one input x. The circuit is described by the following flip-flop input equations: $J_A = x$ $K_A = B'$
$J_B = x$ $K_B = A$.
i) Derive the state equations A (t+1) and B(t+1) by substituting the input equations for the J and K variables.
ii) Draw the state diagram of the circuit. [7+8]

6.a) Draw the block diagram of 4 bit universal shift register using D flip-flops and a 4 ×1 multiplexers. Write the HDL behavioral description of a 4-bit shift register.

b) Draw the logic diagram of a 4bit binary ripple down counter using:
i) flip-flops that trigger on the positive edge of the clock and
ii) flip-flops that trigger on the negative edge of the clock. [7+8]

7.a) Design a combinational circuit using a ROM that accept a 3-bit number and generates an output binary equal to the square of the input number.

b) What are sequential programmable devices? Draw the sequential programmable logic for a basic microcell logic. [7+8]

8.a) Explain the difference between asynchronous and synchronous sequential circuits.

b) Draw the block diagram of an asynchronous sequential circuit and explain its working.

c) Explain the hazards in combinational circuits by taking examples of AND-OR circuit and NAND circuit. [5+5+5]

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