R13

Code No: 5157B

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

M. Tech I Semester Examinations, October - 2015

VLSI TECHNOLOGY AND DESIGN

(VLSI System Design/VLSI Design)

Time: 3hrs **Max.Marks:60**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 20 marks. Answer all questions in Part A.
Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 8 marks and may have a, b, c as sub questions.

PART - A

5 × 4 Marks = 20

1.a) Explain the differences between CMOS and BICMOS inverter circuits. [4]
b) Design the CMOS NOR schematic circuit diagram. [4]
c) Explain power optimization of combinational logic networks. [4]
d) Explain the various testing approaches of VLSI design. [4]
e) Explain the importance of floor plan in VLSI design. [4]

PART - B

5 × 8 Marks = 40

2.a) Design and explain PMOS inverter with schematic circuit.
b) Derive the I_{ds}-V_{ds} relation of CMOS in non-saturation region. [4+4]

OR

3.a) Explain CMOS Fabrication process with neat illustrations.
b) Explain MOS transistor transconductance g_m and output conductance g_{ds}. [4+4]

4.a) Design and explain the XOR schematic circuit.
b) Explain the difference between wires and vias. [4+4]

OR

5.a) Design and explain OR layout with design rules.
b) Explain the 'λ' based design rules. [4+4]

6. Explain fan out reduction by buffer insertion method. [8]

OR

7. Derive the transistor sizing for the following efforts with an example like branching effort and path delay. [8]

8. Design and explain a razor latch. [8]

OR

9. Design and explain the structure of an LSSD latch. [8]

10. Explain the floor plan type of windmill structure introduce irresolvable constraints on routing order and sliceable floor plan. [8]

OR

11. Explain the interconnect properties and wiring plans. [8]

---oo0oo---