Code No: 5157N **R13**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
M. Tech II Semester Examinations, October - 2015
DESIGN FOR TESTABILITY
(VLSI System Design/VLSI Design)

Time: 3 Hours **Max. Marks: 60**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 20 marks. Answer all questions in Part A.
Part B consists of 5 Units. Answer any one full question from each unit.
Each question carries 8 marks and may have a, b, c as sub questions.

PART - A

5 × 4 marks = 20

1.a) Explain the difference between Error, Fault and Failure. [4]
b) Comment on significance of controllability and observability with regard to ATPG Algorithms. [4]
c) Very briefly explain the combinational SCOAP measures. [4]
d) List and very briefly discuss the BIST Pattern Generation Techniques. [4]
e) List the motivations behind Boundary Scan. [4]

PART - B

5 × 8 marks = 40

2. Explain the significance of below listed fault models:
a) Logic and Memory Faults,
b) Bridging Fault
c) Cross-point Fault. [3+3+2]

OR

3. Explain the VLSI technology trend in testing with regard to:
a) At-Speed testing
b) ATE cost and
c) Electromagnetic Interference. [3+2+3]

4. Explain and compare Compiled Code simulation Verses Event Driven Simulation. [8]

OR

5.a) Write about the significance of 5-valued logic states.
b) Explain multiple delay fault and minmax delay fault with an example. [4+4]

6. Compute the combinational SCOAP testability measures (both controllability and observability.) for logic function $Y = ((A+B) \oplus E) + (B \cdot C) + D$. [8]

OR

7. Write short notes on:
a) Significance of Scan Design,
b) Scan design Rules and
c) Phases of testing Scan Circuits. [3+2+3]

8. With neat figures explain the BIST process and implementation with BILBOs.[8]

OR

9. Discuss the advantages and disadvantages of using the BILBO, modified BILBO (MBILBO), and concurrent BILBO (CBILBO) approaches for testing a pipeline-oriented circuit, from the points of view of hardware cost, test time, and fault coverage. [8]

10. Explain the functioning of TAP controller with help of a State diagram. List the functioning of JTAG Test Access Ports. [8]

OR

11. With neat figures explain the operation of Boundary Scan Cell, Boundary Scan Register and Boundary Scan Architecture for external test. [8]

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