Code No: 113BS

R13

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
B.Tech II Year I Semester Examinations, December-2014
DIGITAL LOGIC DESIGN
(Computer Science and Engineering)

Time: 3 Hours **Max. Marks: 75**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 25 marks. Answer all questions in Part A.
Part B consists of 5 Units. Answer any one full question from each unit.
Each question carries 10 marks and may have a, b, c as sub questions.

Part- A **(25 Marks)**

1.a)	What are the simplest technique for detecting errors?	[2M]
b)	What are the basic operations in Boolean algebra?	[3M]
c)	What is race around condition? How it is avoided?	[2M]
d)	What is maxterm?	[3M]
e)	What is a ripple carry-adder?	[2M]
f)	What is a priority encoder?	[3M]
g)	What is a full modulus counter?	[2M]
h)	What are the various methods used for triggering flip-flops?	[3M]
i)	What are types of ROM?	[2M]
j)	What is PLA?	[3M]

Part- B **(50 Marks)**

2.a) Covert 105.15_{10} to binary, octal, hexadecimal.
b) What is hamming code? How is the hamming code word tested and corrected.

OR

3.a) Simplify the following Boolean expressions using the Boolean theorems.
i) (A+B+C) (B'+C) + (A+D) (A'+C)
ii) (A+B) (A+B') (A'+B)
b) Why a NAND and NOR gates are known as universal gates? Simulate all the gates.

4.a) Simplify $Y = \sum m(3, 6, 7, 8, 10, 12, 14, 17, 19, 20, 21, 24, 25, 27, 28)$ using K-map method.
b) Obtain
i) minimal SOP and
ii) minimal POS expressions for the following function
$F(A, B, C, D) = \sum m(0, 1, 5, 8, 9, 10)$

OR

5. Obtain the minimal SOP expression for the switching function using k-map.
$Y = \sum m(1, 5, 7, 13, 14, 15, 17, 18, 21, 22, 25, 29) + \sum d(6, 9, 19, 23, 30)$
Draw and explain the logic diagram.

6.a) Draw the schematic diagram and truth table for full adder. Explain the design approach for full adder using universal gates. Draw the relevant logic diagrams with necessary expressions.

b) Draw and explain the operation of 2's complement adder-subtractor.

OR

7.a) Explain the differences between a MUX and a DEMUX. Realize 16-input multiplexer by cascading of two 8-input multiplexers 74151.

b) Realize the function $f(A, B, C, D) = \prod(1, 4, 6, 10, 14) + d(0, 8, 11, 15)$ using i) 16:1 MUX ii) 8:1 MUX.

8.a) What is meant by 'edge triggered'? Differentiate SR-FF and JK-FF with their functional operation and excitation tables.

b) Draw and explain the circuit diagram of positive edge triggered J-K flip-flop using NOR gates with its truth table. How race around conditions are eliminated?

OR

9.a) Discuss about synchronous and ripple counters. Compare their merits and demerits.

b) What do you mean by universal shift register? Draw and explain its circuit diagram and operation.

10.a) Tabulate the PLA programming table for the following Boolean functions.

$A(x, y, z) = \sum m(0, 2, 3, 7)$

$B(x, y, z) = \sum m(1, 3, 4, 6)$

$C(x, y, z) = \sum m(1, 4)$

Draw and explain the relevant logic diagram.

b) Design, draw and explain 128 × 8 ROM using 32×8 ROM.

OR

11.a) Using PLA logic, implement a BCD to excess-3 code converter. Draw and explain its truth table and logic diagram.

b) Explain in brief, about logic construction of 32×4 ROM. Draw and explain the relevant logic diagram.

---oo0oo---