R09

Code No: 09A40403

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY, HYDERABAD
B.Tech II Year II Semester Examinations, November / December-2013
PULSE AND DIGITAL CIRCUITS
(Common to ECE, BME, ETM)

Time: 3 hours **Max. Marks: 75**

Answer any five questions
All questions carry equal marks

1.a) Derive an expression for the output of a high pass circuit excited by a ramp input.
b) A 1 KHz square wave output from an amplifier has rise time tr = 250 ns and tilt = 10%, determine the upper and lower frequencies. [8+7]

2.a) Explain the response of the clamping circuit when a square wave input is applied under steady state conditions.
b) Explain the effect of diode characteristics on clamping voltage. [8+7]

3.a) Sketch neatly the waveforms of current & voltages for a transistor switch with capacitance loading circuit.
b) What are catching diodes? [11+4]

4.a) Design an astable multivibrator to generate a 5 KHz square wave with a duty cycle of 60% and amplitude 12V. Use NPN silicon transistors having $h_{FE(min)} = 70$, $V_{CE(sat)} = 0.3V$, $V_{BE(sat)} = 0.7V$, $V_{BE(cutoff)} = 0V$ and $R_C = 2K\Omega$. Draw the waveforms seen at both collectors and bases.
b) Explain the operation of bistable multivibrator circuit with circuit diagram and waveform. [8+7]

5.a) Write the differences between the voltage and current time base generators?
b) Draw the circuit diagram and waveforms of a transistor bootstrap time base generator and explain principle of operation. [6+9]

6.a) Draw the circuit of an emitter-coupled bidirectional sampling gate and explain.
b) What is Pedestal? How pedestal can be reduced in a sampling gate circuit? [8+7]

7.a) Explain the principle of 'synchronization' and 'synchronization with frequency division'.
b) Explain the method of pulse synchronization of relaxation devices, with examples. [7+8]

8.a) Draw the OR gate using diodes and resistors. Verify its truth table.
b) Draw a TTL NAND gate and explain its operation. [7+8]

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