Code No: RR210203 | RR | SET-1

B.Tech II Year - I Semester Examinations, May-June, 2012
SWITCHING THEORY AND LOGIC DESIGN
(COMMON TO CSE, EEE, ECE, IT)

Time: 3 hours **Max. Marks: 80**

Answer any five questions
All questions carry equal marks

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1. a) Divide $(101101)_2$ by $(110)_2$
   b) Subtract 12 from 48 using 8 – bit 2's complement arithmetic.
   c) Convert $(5C7)_{16}$ to decimal
   d) Convert $(3956)_{10}$ to octal
   e) Encode data bits 1101 into 7 bit even parity Hamming code. [16]

2.a) Reduce the following
   i) $AB + A(B + C) + \bar{B}(B + D)$
   ii) $A + B + \bar{A}\bar{B}C$
   b) Convert $A(\bar{A} + B)(\bar{A} + B + \bar{C})$ to Canonical POS form.
   c) Convert $\bar{A} + \bar{B}C$ to Canonical SOP form. [16]

3.a) Reduce the following using K- Map.
   $f(w, x, y, z) = \sum m(0,1,2,3,5,7,8,9,10,12,13)$
   $f(A, B, C, D) = \bar{A} + AB + AB\bar{D} + A\bar{B}\bar{D} + C$
   b) i) Draw the logic diagram using only two input – NAND gates to implement the following expression.
   $F = (AB + \bar{A}\bar{B})(C\bar{D} + \bar{C}D)$.
   ii) Write the properties of EX – OR gates. [16]

4.a) Implement the following function using 8×1 Multiplex
   $f(A, B, C, D) = \sum(0,3,4,6,8,10,11,13,15)$
   b) Design Two bit comparator using two one bit comparators.
   c) Give the logic implementation of a 8×4 bit ROM using a decoder of a suitable size. [16]

5.a) Compare combinational and sequential circuits.
   b) What is race around condition in J-K flip flop? How do you eliminate it?
   c) Distinguish between synchronous and Asynchronous sequential circuits. [16]

6.a) Design a sequence detector which produces an output 1 is whenever the sequence 0101 is detected and an output 0 at all other times.
   b) Design a modulo – 6 synchronous counter. [16]

7.a) Distinguish between Moore and Melay machines.
   b) Explain the Capabilities and Limitations of finite state Machines. [16]

8. Write a brief note on
   i) ASM chart
   ii) Threshold Logic [16]

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Code No: RR210203 | RR | SET-2

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b) i) Draw the logic diagram using only two input – NAND gates to implement the following expression.
$F = (AB + \bar{A}\bar{B})(C\bar{D} + \bar{C}D)$.
ii) Write the properties of EX – OR gates. [16]

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$f(A,B,C,D) = \sum(0,3,4,6,8,10,11,13,15)$

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c) Convert $\bar{A} + \bar{B}C$ to Canonical SOP form. [16]

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Code No: RR210203 | RR | SET-3

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SWITCHING THEORY AND LOGIC DESIGN
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Time: 3 hours **Max. Marks: 80**

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Code No: RR210203 | RR | SET-4

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