Code No: R09221902 | R09 | SET-1

B.Tech II Year - II Semester Examinations, April-May, 2012
ANALOG AND DIGITAL IC APPLICATIONS
(Electronics and Computer Engineering)

Time: 3 hours **Max. Marks: 75**

Answer any five questions
All questions carry equal marks

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1.a) Classify the Integrated Circuits based on device used, chip complexity, chip size and application.

b) An amplifier using an op-amp with slew-rate, SR = 1V/μsec has a gain of 40dB. Estimate the maximum peak-to-peak amplitude of input signal for this amplifier to faithfully amplify sinusoidal signals from DC to 20 KHz without introducing any slew-rate induced distortion.

c) Explain the concept of "Virtual Ground" in op-amps. [5+6+4]

2.a) In the op-amp circuit shown in Figure.1, estimate the output voltage, V_{out}.

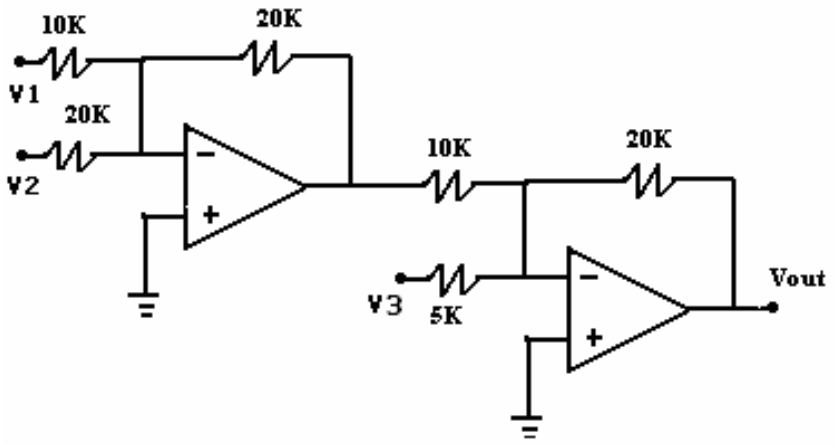

Figure.1

b) In the op-amp Schmitt trigger circuit shown in Figure.2, estimate the lower and upper threshold voltage levels. Also calculate the hysteresis voltage. [8+7]

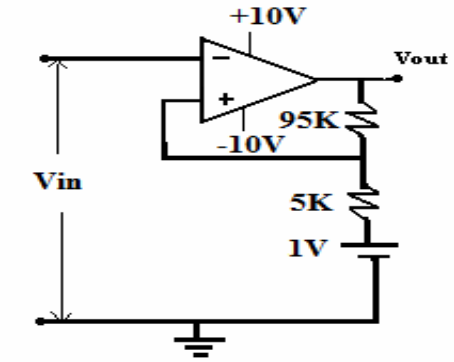

Figure.2

3.a) Draw the circuit of Delay equalizer and explain its operation. Also derive expression for its transfer function.

b) Draw the circuit of Wein-bridge oscillator using op-amp and explain its operation. Also derive expression for frequency of oscillations. [7+8]

4.a) Explain the application of PLL as frequency multiplier and AM demodulator.

b) Design an astable multivibrator using 555 timer to operate at 5 KHz with duty cycle of 0.6 and timing capacitor of 0.1μF. What modifications do you propose to get 50% duty cycle from the above mentioned circuit? [7+8]

5.a) With a neat block diagram and timing diagrams, explain the operation of an 8-bit successive approximation ADC. Comment on its conversion speed with respect to the speeds of parallel ADC and dual slope ADC.

b) An 8-bit DAC has a full scale output voltage of 20V. If the digital input to the converter is 11011011, estimate the output voltage and % resolution. [10+5]

6.a) Draw the circuit of a 2-input TTL totempole output NAND gate with the help of four transistors. Explain why the output of this gate cannot be wired-ANDed.

b) Explain the function of multi emitter transistor used in the circuit. What is the disadvantage of using back to back diodes in place of multi emitter transistor?

c) Explain why this logic circuit is faster than open collector logic circuit? [6+6+3]

7. Implement a 32-input to 5-output priority encoder using four 74LS148 ICs and explain. [15]

8.a) What type of inputs does a clocked Flip-flop have? Explain. What is meant by edge-triggering? Define set-up time and hold-time for clocked FF.

b) Explain the dynamic RAM structure. [9+6]

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Time: 3 hours **Max. Marks: 75**

Answer any five questions
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- - -

1.a) Draw the pin diagram of µA741 op-amp and explain the function of each pin. Also list its important features.

b) An operational amplifier with CMRR = 1000 has inputs, V_1 = 1050µV and V_2 = 950µV. Find the percentage error in the differential output? [8+7]

2.a) In the op-amp circuit shown in Figure.1, obtain an expression for the current, I3.

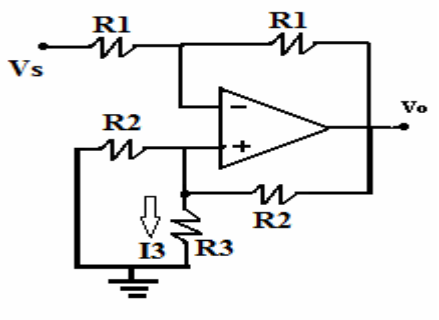

Figure.1

b) Draw the circuit of inverting integrator using an ideal op-amp with R = 50Ω, C = 0.1µF and a supply voltage of ±15V. Explain its operation with necessary equations. Also calculate its output voltage after 0.5msec of the application of a step input voltage of 50mV. [7+8]

3.a) Obtain the transfer function of the active filter circuit shown in Figure.2. Also estimate the 3dB frequency, if C = 0.1µF, R1 = 2KΩ and R2 = 10KΩ.

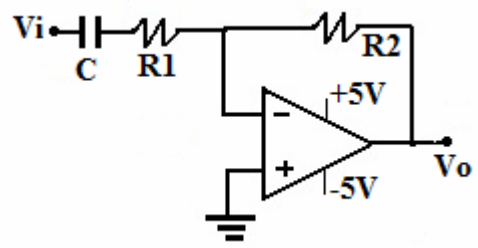

Figure.2

b) Draw the functional block diagram of VCO. With necessary expressions, explain how it generates square and triangular wave forms. [7+8]

4.a) Explain the application of PLL as frequency translator and FM demodulator.

b) Explain the application of 555 timer as Schmitt trigger and FSK generator. [7+8]

5.a) Draw and explain the operation of dual-slope ADC. Explain why it is preferred in a digital voltmeter.

b) A certain D/A converter has the lowest and highest values of resistances 1KΩ and 8KΩ respectively. If the bit length of the converter is increased by 2, estimate the number of additional resistors required and their values. [8+7]

6.a) Which is the fastest non-saturated logic family? With a neat circuit diagram explain its operation in view of logic of operation, noise margin, propagation delay and fan-out.

b) In 4-input NAND gate, two inputs are to be used. What are the options available for the unused inputs and which one is the best and why? [10+5]

7. Design an 8-bit BCD adder using IC74283 and explain its operation in detail. [15]

8.a) What is ROM? Write the truth table of a 2 to 4 decoder with output polarity control and built with discrete gates and with an 8 × 4 ROM.

b) Distinguish between combinational circuits and sequential circuits. [9+6]

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Time: 3 hours **Max. Marks: 75**

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1.a) Explain at least five major electrical characteristics (both AC & DC) of an op-amp.

b) An amplifier using an op-amp with slew-rate, SR = 0.5V/µsec has a gain of 40dB. Estimate the maximum frequency of a sinusoidal input signal of peak value, 2V rms that can be handled without excessive distortion. [10+5]

2.a) Estimate the output voltage (Vo), in the non-inverting summing amplifier circuit using op-amp, shown in Figure.1.

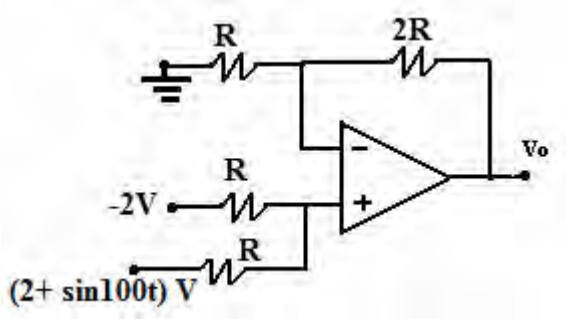

Figure.1

b) Draw the circuit diagram and explain the operation of series voltage regulator using op-amp. Derive an expression for its output voltage. [7+8]

3.a) Explain the operation of the op-amp oscillator circuit shown in Figure.2. What type of signal does it produce? Derive the expression for its frequency of oscillation.

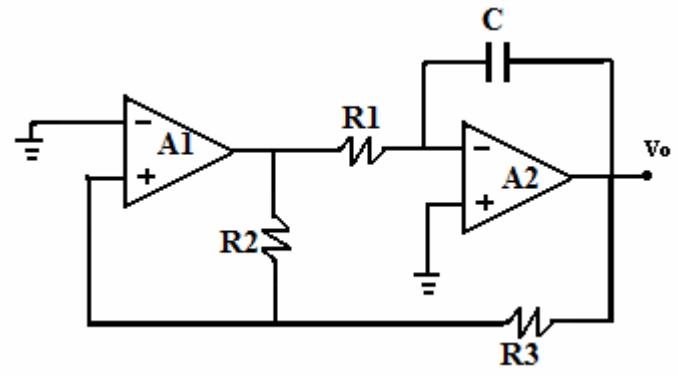

Figure.2

b) Design a multiple feedback active narrow band pass filter with the following specifications: Central frequency (f_C) = 1.5 KHz, Quality factor (Q) = 7, pass band gain (A_f) = 15 and C1 = C2 =0.02µF. [9+6]

4.a) Draw the block diagram of PLL. Explain the function of each block.

b) With neat sketches, explain the operation of Astable multivibrator using 555 timer and derive expression for its frequency of oscillations. [7+8]

5.a) Draw and explain the operation of R-2R ladder DAC. Also derive expression for its output voltage.

b) An 8-bit successive approximation ADC used a clock frequency of 1MHz. Calculate the conversion time of the converter. [10+5]

6.a) Design a 2-input AND gate using CMOS transistors. Explain the operation of the circuit with the help of function table.

b) What is meant by tri-state logic? Draw the circuit of tri-state TTL logic and explain its operation in detail. [8+7]

7. Design a 4 to 16 decoder using two 74LS138 (3-to-8 decoder) ICs. Explain its operation with the help of function table. [15]

8.a) Explain how a D flip-flop can be implemented using JK flip-flop.

b) What are the various categories of semiconductor memories? Compare them based on access time, power requirements, cost per bit, noise immunity and packing density. [8+7]

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Time: 3 hours **Max. Marks: 75**

Answer any five questions
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- - -

1.a) Explain the three basic modes of operation and possible applications using an open-loop ideal op-amp.

b) An operational amplifier has inputs, V_1 = 1050μV and V_2 = 950μV. Estimate the CMRR required to get a differential output with not more than 1% error. [8+7]

2.a) In the op-amp circuit shown in Figure.1, the diode current, $I = I_s(e^{V/V_T})$.
For V_i = 2V, $V_O = V_{O1}$ and for V_i = 4V, $V_O = V_{O2}$.
Then show that $V_{O1} - V_{O2} = V_T \ln 2$.

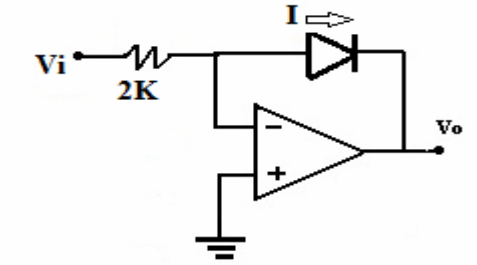

Figure.1

b) Draw and explain the need of sample & hold circuit. With reference to the sample & hold circuit, define: Aperture time, Aperture uncertainty, Hold mode settling time and Feedthrough. [7+8]

3.a) Design a Butterworth active low pass filter for given normalized polynomial of $S^2 + 1.414\,S + 1$.

b) "To implement a phase-shift oscillator practically, minimum three identical RC high pass sections are to be cascaded". Justify. Draw one such phase-shift oscillator using op-amp and derive expression for its frequency of oscillations. [7+8]

4.a) Draw the functional block diagram of IC565 PLL. Derive expressions for lock-in range and capture range.

b) It is desired to display the train information such as train number, time of arrival and platform number on a digital display board in a railway station, immediately after pressing a push button and the information is to be displayed for a period of 60 seconds. Design and construct an electronic circuit using 555 timer with 100μF timing capacitor. [8+7]

5.a) Draw the circuit of an 8-bit Digital to Analog Converter (DAC) using 741 op-amp. The output voltage of the converter corresponding to full-scale input is 5.0V, when a reference voltage of 2.5V is applied. If the value of the weighted resistor corresponding to MSB is 1KΩ, design the values of remaining resistors used in the circuit. What should be the tolerance of the resistor corresponding to MSB, if the error in the converter output is to remain less than 1% of full scale value.

b) Arrange the following A/D converters in order of increasing speed of operation:
i) Successive approximation ADC ii) Dual-slope ADC
iii) Flash-type ADC iv) single-slope ADC. [12+3]

6.a) Draw the model of a CMOS inverter and explain its behavior for LOW and HIGH inputs.

b) What is meant by active pull-up? Draw the circuit of TTL active pull-up NAND gate and explain its operation with the help of function table. [7+8]

7. Design an 8-bit comparator using two 7485 ICs. Explain its operation with the help of function table. [15]

8. Design a 4-bit bi-directional universal shift register using 74LS194IC. Explain its operation with the help of block diagram and timing diagram. [15]

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