Code No: R09220204 | R09 | SET-1

B.Tech II Year - II Semester Examinations, April-May, 2012
SWITCHING THEORY AND LOGIC DESIGN
(Common to EEE, ECE, ETM, BME)

Time: 3 hours **Max. Marks: 75**

Answer any five questions
All questions carry equal marks

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1.a) Convert the number $(17.125)_{16}$ to base 10, base 4, base 5 and base 2.
b) Perform the binary arithmetic operations on (-14)-(-2) using signed 2's complement representation.
c) Justify the statement that "Gray code is a class of reflected code". [6+6+3]

2.a) State and Prove De Morgan's theorem of Boolean Algebra.
b) Determine the canonical product-of-sums and sum-of-products form of T(x,y,z) = x'(y' + z')
c) Realize the basic gates using NAND and NOR gates only. [5+ 4+6]

3.a) Prove that if w'x + yz' = 0, then wx + y'(w' + z') = wx + xz + x'z' + w'y'z.
b) For the given function T(w,x,y,z) = ∑ (0,1,2,3,4,6,7,8,9,11,15)
i) Show the map
ii) Find all prime implicants and indicate which are essential.
iii) Find a minimal expression for T and realize using basic gates. Is it unique? [7+8]

4.a) Design a 2-bit comparator which compares the magnitude of two numbers X and Y and generates three output f1,f2, and f3.
b) Realize 16 × 1 Mux using only 2 × 1 Mux. [8+7]

5.a) Realize the given function using PLD circuit.
F(x,y,z) = xy + yz + x'y' .
b) What is meant by Logic simulation, Functional simulation, timing simulation and Logic synthesis? [9+6]

6.a) Design a BCD counter using JK Flip-Flops.
b) Write the differences between synchronous and asynchronous counters.
c) Draw the state diagram and characteristic table of Master Slave JK flip-flop. [8+3+4]

7.a) Write the differences between completely specified function and incompletely specified functions with examples.
b) Design an asynchronous sequential circuit with two inputs X and Y and with one output Z. Whenever Y is 0, input X is transferred to Z, otherwise, the output remains same. [6+9]

8.a) Differentiate between Mealy and Moore machine with examples.
b) Write about the implementation of Binary multiplier. [8+7]

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Code No: R09220204 | R09 | SET-2

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SWITCHING THEORY AND LOGIC DESIGN
(Common to EEE, ECE, ETM, BME)

Time: 3 hours **Max. Marks: 75**

Answer any five questions
All questions carry equal marks

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1.a) Convert the number $(127.75)_8$ to base 10, base 3, base 16 and base 2.
b) Given that $(64)_{10} = (100)_b$, determine the value of b.
c) Perform the binary arithmetic operations on (+12)-(4) using signed 2'scomplement representation. [5+4+6]

2.a) State and Prove the Huntington postulates of Boolean Algebra.
b) Find the complement of the function and represent in sum of minterms F(x,y,z) = xy + z'
c) Simplify the following function and realize using universal gates
F(A,B,C) = A'BC' + ABC + B'C' + A'B' [5+4+6]

3.a) Use the tabulation procedure to generate the set of prime implicants and to obtain all minimal expressions for the following function
F(a,b,c,d) = ∑ (1,5,6,12,13,14) + ∑d(2,4)
b) For the given function T(w,x,y,z) = ∑ (0,1,5,7,8,10,14,15)
i) Show the map
ii) Find all prime implicants and indicate which are essential.
iii) Find a minimal expression and realize using basic gates. [8+7]

4.a) Design a combinational circuit to find the 2's complement of a given 4bit binary number and realize using NAND gates.
b) Design a full adder using Multiplexer. [8+7]

5.a) What is PAL? How does it differ from PROM and PLA?
b) Design a switching circuit that converts a 4 bit binary code into a 4 bit Gray code using ROM array. [6+9]

6.a) Define Setup and Hold times.
b) Write the characteristic, excitation tables for JK, RS, T and D flip-flops.
c) Design a synchronous counter to generate the sequence 0,1,1,2,3,5,8, and repeat the sequence using T flip-flops. [2+6+7]

7.a) Construct the state diagram and primitive flow table for an asynchronous machine that has two inputs and one output. The input sequence xy = 00, 01, 10 causes the output to become 1. The next input change then causes the output to return to 0. No other inputs will produce a 1 output.
b) Write the usage of merger graph with example. [8+7]

8.a) Write the usage of Mealy machine with example.
b) Discuss the implementation of Binary multiplier with appropriate realizations. [8+7]

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Code No: R09220204 | R09 | SET-3

B.Tech II Year - II Semester Examinations, April-May, 2012
SWITCHING THEORY AND LOGIC DESIGN
(Common to EEE, ECE, ETM, BME)

Time: 3 hours **Max. Marks: 75**

Answer any five questions
All questions carry equal marks
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1.a) Convert the following to the required form.
i) $(A98B)_{12}$ = (---------)$_3$ ii) $(38.65)_{10}$ = (----------)$_2$.
b) Use 2's complement form perform subtraction.
i) 1101010-110100 ii) 10011.1101-101.11 [15]

2.a) Simplify the following
i) $\left(\overline{A}+\overline{AC}+\overline{B}\right)$ ii) $F = AB(C+\overline{C})+A\overline{B}$ iii) $F=\left(\overline{X}+\overline{Y}\right)\left(\overline{X}+\overline{Z}\right)$
b) Prove that NAND and NOR gates are Universal gates. [15]

3.a) Simplify the following function using K-map.
F(A,B,C,D) = $\sum(1,3,4,5,6,11,13,14,15)$
b) Simplify the following using Tabular method.
F(A,B,C,D) = $\sum(3,7,8,12,13,15)+\sum_{\phi}(9,14)$. [15]

4.a) Design a 64:1 MUX using 8:1 MUXs.
b) Design a 4 bit parallel adder using Full adder modules. [15]

5.a) Design a 4-bit parity checker/ generator circuit that can generate even parity using logic gates.
b) Write a brief note on threshold logic synthesis. [15]

6.a) What is meant by clock skew? How to handle it?
b) Explain the term Race around condition. How is it satisfied by Master-slave Flip-Flops. [15]

7.a) Design a modulo 10 counter JK flipflops.
b) What are the rules to develop a Merger chart? [15]

8. Design a binary multiplier and its control logic by drawing ASM chart and realize the same using decoder, MUX and D flipflops. [15]

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Code No: R09220204 | R09 | SET-4

B.Tech II Year - II Semester Examinations, April-May, 2012
SWITCHING THEORY AND LOGIC DESIGN
(Common to EEE, ECE, ETM, BME)

Time: 3 hours **Max. Marks: 75**

Answer any five questions
All questions carry equal marks

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1.a) Develop a Gray code for $(42)_{10}$ and $(97)_{10}$ and convert the same to Hex sequence.
b) Explain different error detecting and correcting codes in digital system. [15]

2.a) Show that i) $\overline{AB + \overline{AB}} = A \oplus B$
ii) $\overline{(A \oplus B)} = (A \odot B)$
b) Reduce the following boolean expressions using theorems and identities.
i) $F = C + AB + AD(B + \bar{C}) + CD$
ii) $F = AB + C\bar{D}B + \bar{A}C\bar{D}$ [15]

3.a) Simplify the following using prime implicant chart method.
f(A,B,C,D) = $\sum(0,5,7,8,9,10,11,13)$
b) Use tabular method and simplify the following 5 variable function
F(A,B,C,D,E) = $\sum(0,4,8,12,16,20,24,28) + \sum_{\phi}(1,5,7,23)$. [15]

4.a) Design a 4 bit comparator circuit using logic gates.
b) Design a code converter logic circuit which converts BCD code to Excess-3 code. [15]

5.a) Design a square generator logic for 4 bit input using ROM.
b) What are the capabilities and limitations of threshold gate? [15]

6.a) Convert RS flip flop to a
i) D-latch ii) T-latch.
b) Design a FSM which detects 0011 pattern and set z = 1 for all other patterns z = 0 [15]

7.a) Design a multi mode universal shift registers of 4 bit.
b) Draw a block diagram of Modulo 10 ripple counter and explain its timing diagram. [15]

8. Design a control logic through ASM Chart for the sequence detector which detects 1100 and resets flip flop F to 0 and flip flop E to 1. The patterns come from 4 bit counter A. [15]

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