R09

Code No: C0601, C5503, C7703, C6803, C5703, C7003, C4507, C3803

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

M.TECH I SEMESTER EXAMINATIONS, APRIL/MAY-2012

VLSI TECHNOLOGY AND DESIGN

(COMMON TO DIGITAL SYSTEMS & COMPUTER ELECTRONICS, EMBEDDED SYSTEMS, EMBEDDED SYSTEMS & VLSI DESIGN, VLSI & EMBEDDED SYSTEMS, VLSI SYSTEM DESIGN, ELECTRONICS & COMMUNICATION ENGINEERING, SYSTEMS & SIGNAL PROCESSING, DIGITAL ELECTRONICS & COMMUNICATION SYSTEMS)

Time: 3hours **Max. Marks: 60**

Answer any five questions
All questions carry equal marks

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1. Draw the circuits for n-MOS, p-MOS and C-MOS Inverter and explain about their operation and compare them.

2.a) Explain about scalable Design rules related to NMOS and CMOS Technologies.
b) What are the issues involved in driving large capacitive loads in VLSI circuits? Explain.

3. Explain the following
a) Why is n-diffusion to p-diffusion spacing is so large?
b) Why metal - metal spacing is larger than ploy-ploy spacing?
c) What are the effects of scaling of V_t?

4.a) Explain how to reduce the cross talk by using ground wire to minimize cross talk.
b) Explain how fan-out and path delay influences delay in combinational networks.

5.a) What are various floor planning methods? Discuss in brief.
b) Explain the delay in combinational logic network and how combinational delay can be reduced.

6.a) What are the various issues in system-on-chip design? Explain it briefly.
b) Develop a sequence of tests for the '01' string recognizer which tests every combinational gate for both stuck -at -0 and stuck -at-1 faults.

7.a) Explain how the extracting a data path and controller from the ASM chart.
b) Explain how would you translate a register transfer structure into a legal two phase latched sequential machine give an example.

8.a) Explain the sequential testing for testing a sequential machine and time-frame expansion of a sequential test.
b) Write short notes on Chip design methodologies.

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