Code No: 07A40401 **R07** **Set No. 2**

II B.Tech II Semester Examinations,April/May 2012
DIGITAL IC APPLICATIONS
Electronics And Instrumentation Engineering

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Generate the truth table for a code converter whose inputs are 4-bit binary numbers (B_3, B_2, B_1, B_0) and outputs are corresponding gray coded numbers (G_3, G_2, G_1, G_0). Gray code can be obtained from binary code by repeating MSB and successive bits by performing EX-OR with previous bits. Write a VHDL code for the code converter.
   (b) Modify the VHDL code for Binary coded Decimal (BCD) inputs. [8+8]
2. Give the Design flow for VHDL Hardware Description language and explain the same. [16]
3. (a) Generate the truth table of a 4-input dual parity generator with a control signal 'Even/odd', such that, the output is even parity if 'Even/odd' = '0' and odd parity otherwise.
   (b) Translate the truth table in to a minimized logic circuit.
   (c) Write a VHDL code to simulate the designed dual parity generator circuit. [16]
4. (a) Differentiate between synchronous binary counters and ripple counters.
   (b) Draw the function table and timing diagram of a 4-bit ripple counter.
   (c) Write a VHDL program to simulate a 4-bit ripple counter. [16]
5. Design a 10 to 4 encoder with inputs 1out of 10 code and outputs in BCD? Write the VHDL program using data flow modeling. [16]
6. (a) Compare and contrast commercially available Read only memories, PROM, EPROM and EEPROM.
   (b) Realize a 3-to-8 decoder circuit using an appropriate sized MOS transistor based Read Only Memory. [8+8]
7. (a) Draw the circuit diagram of a two-input LS-TTL NOR gate and explain the functional behavior.
   (b) Mention the DC noise margin levels of ECL 10K family. [8+8]
8. (a) What is meant by logic family? Classify various types of logic families.
   (b) Explain the operation of nMOS and pMOS transistors. [8+8]

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Code No: 07A40401 **R07** **Set No. 4**

II B.Tech II Semester Examinations,April/May 2012
DIGITAL IC APPLICATIONS
Electronics And Instrumentation Engineering

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Generate the truth table of a 4-input dual parity generator with a control signal 'Even/odd', such that, the output is even parity if 'Even/odd' = '0' and odd parity otherwise.
   (b) Translate the truth table in to a minimized logic circuit.
   (c) Write a VHDL code to simulate the designed dual parity generator circuit. [16]

2. (a) Differentiate between synchronous binary counters and ripple counters.
   (b) Draw the function table and timing diagram of a 4-bit ripple counter.
   (c) Write a VHDL program to simulate a 4-bit ripple counter. [16]

3. Design a 10 to 4 encoder with inputs 1out of 10 code and outputs in BCD? Write the VHDL program using data flow modeling. [16]

4. (a) What is meant by logic family? Classify various types of logic families.
   (b) Explain the operation of nMOS and pMOS transistors. [8+8]

5. (a) Draw the circuit diagram of a two-input LS-TTL NOR gate and explain the functional behavior.
   (b) Mention the DC noise margin levels of ECL 10K family. [8+8]

6. (a) Compare and contrast commercially available Read only memories, PROM, EPROM and EEPROM.
   (b) Realize a 3-to-8 decoder circuit using an appropriate sized MOS transistor based Read Only Memory. [8+8]

7. (a) Generate the truth table for a code converter whose inputs are 4-bit binary numbers (B_3, B_2, B_1, B_0) and outputs are corresponding gray coded numbers (G_3, G_2, G_1, G_0). Gray code can be obtained from binary code by repeating MSB and successive bits by performing EX-OR with previous bits. Write a VHDL code for the code converter.
   (b) Modify the VHDL code for Binary coded Decimal (BCD) inputs. [8+8]

8. Give the Design flow for VHDL Hardware Description language and explain the same. [16]

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Code No: 07A40401 **R07** **Set No. 1**

II B.Tech II Semester Examinations,April/May 2012
DIGITAL IC APPLICATIONS
Electronics And Instrumentation Engineering

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Generate the truth table of a 4-input dual parity generator with a control signal 'Even/odd', such that, the output is even parity if 'Even/odd' = '0' and odd parity otherwise.
   (b) Translate the truth table in to a minimized logic circuit.
   (c) Write a VHDL code to simulate the designed dual parity generator circuit. [16]

2. (a) Generate the truth table for a code converter whose inputs are 4-bit binary numbers (B_3, B_2, B_1, B_0) and outputs are corresponding gray coded numbers (G_3, G_2, G_1, G_0). Gray code can be obtained from binary code by repeating MSB and successive bits by performing EX-OR with previous bits. Write a VHDL code for the code converter.
   (b) Modify the VHDL code for Binary coded Decimal (BCD) inputs. [8+8]

3. Give the Design flow for VHDL Hardware Description language and explain the same. [16]

4. (a) Compare and contrast commercially available Read only memories, PROM, EPROM and EEPROM.
   (b) Realize a 3-to-8 decoder circuit using an appropriate sized MOS transistor based Read Only Memory. [8+8]

5. (a) Draw the circuit diagram of a two-input LS-TTL NOR gate and explain the functional behavior.
   (b) Mention the DC noise margin levels of ECL 10K family. [8+8]

6. (a) Differentiate between synchronous binary counters and ripple counters.
   (b) Draw the function table and timing diagram of a 4-bit ripple counter.
   (c) Write a VHDL program to simulate a 4-bit ripple counter. [16]

7. (a) What is meant by logic family? Classify various types of logic families.
   (b) Explain the operation of nMOS and pMOS transistors. [8+8]

8. Design a 10 to 4 encoder with inputs 1out of 10 code and outputs in BCD? Write the VHDL program using data flow modeling. [16]

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Code No: 07A40401 **R07** **Set No. 3**

II B.Tech II Semester Examinations,April/May 2012
DIGITAL IC APPLICATIONS
Electronics And Instrumentation Engineering

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Generate the truth table of a 4-input dual parity generator with a control signal 'Even/odd', such that, the output is even parity if 'Even/odd' = '0' and odd parity otherwise.
   (b) Translate the truth table in to a minimized logic circuit.
   (c) Write a VHDL code to simulate the designed dual parity generator circuit. [16]

2. (a) Differentiate between synchronous binary counters and ripple counters.
   (b) Draw the function table and timing diagram of a 4-bit ripple counter.
   (c) Write a VHDL program to simulate a 4-bit ripple counter. [16]

3. (a) Compare and contrast commercially available Read only memories, PROM, EPROM and EEPROM.
   (b) Realize a 3-to-8 decoder circuit using an appropriate sized MOS transistor based Read Only Memory. [8+8]

4. (a) What is meant by logic family? Classify various types of logic families.
   (b) Explain the operation of nMOS and pMOS transistors. [8+8]

5. Give the Design flow for VHDL Hardware Description language and explain the same. [16]

6. (a) Generate the truth table for a code converter whose inputs are 4-bit binary numbers (B_3, B_2, B_1, B_0) and outputs are corresponding gray coded numbers (G_3, G_2, G_1, G_0). Gray code can be obtained from binary code by repeating MSB and successive bits by performing EX-OR with previous bits. Write a VHDL code for the code converter.
   (b) Modify the VHDL code for Binary coded Decimal (BCD) inputs. [8+8]

7. (a) Draw the circuit diagram of a two-input LS-TTL NOR gate and explain the functional behavior.
   (b) Mention the DC noise margin levels of ECL 10K family. [8+8]

8. Design a 10 to 4 encoder with inputs 1out of 10 code and outputs in BCD? Write the VHDL program using data flow modeling. [16]

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