Code No: 53024 **R09**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY, HYDERABAD
B.Tech II Year I Semester Examinations, May/June - 2015
DIGITAL LOGIC DESIGN
(Computer Science and Engineering)

Time: 3 hours **Max. Marks: 75**

Answer any five questions
All questions carry equal marks

- - -

1.a) What do you mean by Gray code? What are its applications? Give some examples.

b) Convert the following
i) $(977)_{10} = (?)_{16}$
ii) $(657)_{10} = (?)_{8}$
iii) $(754)_{10} = (?)_{2}$
iv) $(1001)_{16} = (?)_{10}$ [7+8]

2.a) State and prove De'Morgans theorem.

b) Prove that:
$(\bar{A}+\bar{B}+\bar{D})(\bar{A}+B+\bar{D})(B+C+D)(A+\bar{C})(A+\bar{C}+D) = \bar{A}\bar{C}D+AC\bar{D}+B\bar{C}\bar{D}$ [7+8]

3.a) Write the map entered variable K-Map for the Boolean function
$f(w,x,y,z) = \sum m(2,9,10,11,13,14,15)$.

b) Design a 2 input XOR and XNOR using NAND and NOR gates respectively by using only 4 gates each. [8+7]

4.a) Implement the following Boolean function using 8:1 multiplexer
$f(A,B,C,D) = \bar{A}B\bar{D} + ACD + \bar{B}CD + A\bar{C}D$.

b) What is a decoder? Construct a 4×16 decoder with two 3×8 decoders. [7+8]

5.a) Write the HDL behavioral description of a D-Flip Flop.

b) Draw the circuit of a JK- Flip Flop using NAND gates. What type of problem is encountered in this type of Flip Flop? Explain the methods to overcome it. [7+8]

6.a) Design a synchronous counter using D-FlipFlop with the repeated binary sequence 0,1,2,4,5,6.

b) Design a 4-bit universal shift register and explain its operation. [8+7]

7. Give the PLA realization of the given functions using a PLA with 6 inputs, 4 outputs and 10 AND gates.
$F_1(A,B,C,D,E,F) = \sum m\ (0,1,2,3,7,8,9,10,11,15,32,33,34,35,39,40,41,42,43,45,47)$
$F_2(A,B,C,D,E,F) = \sum m\ (8,9,10,11,12,14,21,25,27,40,41,42,43,44,46,57,59)$.
[15]