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Code No: A5505

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
M.TECH. I SEMESTER EXAMINATIONS, APRIL/MAY-2012
ANALOG AND DIGITAL IC DESIGN
(EMBEDDED SYSTEMS)

Time: 3 hours **Max. Marks.60**

Answer any Five Questions
All questions carry equal marks

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1.a) Draw the circuit diagram of two stage CMOS op amp and explain how to design it.
b) Explain how the large area ratio caused by unequal mirror currents can be avoided by widler BJT current mirror circuit?

2.a) Explain how a PLL is used for clock recovery in receiver ?
b) How a filter can be designed using a switched capacitor integrators?

3.a) How to interface the CMOS and TTL logic family gates?
b) Design a multiplexer circuit for a 4-bit and write a VHDL program for it.

4.a) Design a peak detector circuit using switched capacitor.
b) Write a VHDL program for a shift register and draw the corresponding logic diagram.

5.a) Draw the typical memory chip architecture and explain it.
b) What are the basic building blocks for a digital single bit adder and explain the function of each block.

6.a) Compare the CPLD and FPGA with respect to design of the digital system.
b) Draw the architecture of XC9500 CPLD family and explain the internal architecture of CLB of it.

7.a) Given a digital word to be converted is 11001 in the order of MSB to LSB and find the analog value of this digital word in terms of V_{ref}.
b) Explain the principle of operation of latched comparator.
c) Draw the circuit diagram of successive approximation A/D converter and explain it.

8. Write short notes on the following
a) Types of Noses
b) Parasitic insensitive integrators

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