R09 Code No: R09220403 ... JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY, HYDERABAD B.Tech II Year II Semester Examinations, May-2013 **Pulse and Digital Circuits** (Common to ECE, BME, ETM) Time: 3 hours Max. Marks: 75 Answer any five questions All questions carry equal marks 1.a) Compare linear wave shaping with non-linear wave shaping. A symmetrical square wave of peak-to-peak amplitude 'V' and frequency 'f' is applied to a high pass circuit. Show that the percentage tilt is given by $P = \frac{1 - e^{-1/2RCf}}{1 + e^{-1/2RCf}} \times 100\%$ [7+ [7+8]2.a) Explain the response of the clamping circuit when a square wave input is applied under steady state conditions. ::: b) Explain the effect of diode characteristics on clamping voltage, 3. Write short notes on: a) Diode switching times b) Switching characteristics of transistors c) FET as a switch. *** What is a monostable multivibrator? Explain with the help of a neat circuit diagram the principle of operation of a monostable multivibrator, and derive an expression for pulse width. Draw the wave forms at collector and base of both transistors. [15] ...5.a) Why the time base generators are called sweep circuits? Write the differences between the voltage and current time base generators? b) With neat sketches and necessary expressions, explain the transistor Miller time-base generator. [9+6]With the help of a neat diagram, explain the working of four-diode sampling *** gate. Derive expressions for its gain(A) and V b) Explain the application of sampling gate in a sampling scope. [10+5]7.a)With the help of a neat circuit diagram and waveforms explain synchronization of a sweep generator with pulse signals. Compare sine-wave synchronization with pulse synchronization. ...: i**. 8.a)

Realize a three-input NAND gate using Transistor Transistor Logic. Explain its operation with Totem-pole load.

b) With reference to logic gates, explain the terms:

(i) Fan-out, (ii) Noise Margin, (iii) Propagation Delay, (iv) Figure of Merit.