R16

Code No: 134CF

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

B.Tech II Year II Semester Examinations, April - 2018

SWITCHING THEORY AND LOGIC DESIGN

(Common to EEE, ECE, MCT)

Time: 3 Hours **Max. Marks: 75**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 25 marks. Answer all questions in Part A.
Part B consists of 5 Units. Answer any one full question from each unit.
Each question carries 10 marks and may have a, b, c as sub questions.

PART- A

(25 Marks)

1.a) What is self complementing code? Give example. [2]
b) State and Prove Demorgan's theorem. [3]
c) What are Hazards? List their types. [2]
d) Design 2 × 1 Multiplexer with neat logic diagram. [3]
e) Write the characteristic table of JK Flip flop. [2]
f) Draw the logic diagram of Master-Slave D flip flop. Use NAND gates. [3]
g) What is switch tail ring counter? [2]
h) What is a Ring Counter? What are applications of Ring counters? [3]
i) What is an ASM Block? [2]
j) Define merger graph of n-state machine M. [3]

PART-B

(50 Marks)

2.a) i) Convert the given Octal number $(2564.603)_8$ to Hexadecimal Number.
ii) Given that $(81)_{10} = (100)_b$, Find the value of b.
b) Encode data bits 1101 into 7 bit even parity Hamming Code. [5+5]

OR

3.a) Prove that AB'C + B + BD'+ ABD'+ A'C = B + C.
b) Simplify the following expression F = AB'+ABD+ABD'+A'C'D'+A'BC' and implement with NAND gates. [5+5]

4.a) Design a code converter that converts BCD messages into Excess-3 code. The converter has four input lines carrying signals labeled *w*, *x*, *y* and *z* and four output lines carrying signals *f*1, *f*2, *f*3, and *f*4.
b) Simplify the following Boolean expression using K- map and implement them with NOR logic gates
F(A,B,C,D)= Σ m (1,3,7,11,15) + d(0,2,5) [5+5]

OR

5.a) Design and explain 3 to 8 decoder with necessary truth table and logic diagram.
b) Write short notes on Hazards and Hazard free relations. [5+5]

6.a) Derive the characteristic equation for JK flip-flop and T flip-flop.
b) Distinguish combinational and sequential circuits. [5+5]

OR

7.a) What are the fundamentals of Sequential machine operation?
b) Discuss about binary cell in detail. [5+5]

8.a) Design a 4-bit binary synchronous counter with D flip flops.
b) What are the steps in state reduction? Explain with an example. [5+5]

OR

9.a) Construct a Johnson counter for 10 timing signals.
b) Draw the 4-bit binary ripple counter using flip flops that trigger on positive edge transition. [5+5]

10.a) Draw the Merger Graph and obtain the set of maximum compatibilities for the given incompletely specified sequential machine.

Present State	Next State, Z	
	I_1	I_2
A	E, 0	B, 0
B	F,0	A, 0
C	E, _	C, 0
D	F, 1	D, 0
E	C,1	C,0
F	D,-	B,0

b) Draw the State diagram, State table and ASM chart for a D flip-flop. [5+5]

OR

11.a) Draw the State diagram and ASM chart for sequence detector to detect 1010.
b) We wish to design a sequence detector circuit, which detects three or more consecutive 1's in a string of bits coming through an input line.
i) Find the state diagram.
ii) Determine the type of the circuit (Moore or Mealy model). [5+5]

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