Code No.: R22CS302PC | R22 | H.T.No. | | | 8 | R | | | | | |

CMR ENGINEERING COLLEGE: : HYDERABAD
UGC AUTONOMOUS
II–B.TECH–I–Semester End Examinations (Regular) - December- 2024
COMPUTER ORGANIZATION AND ARCHITECTURE
(Common for CSE, IT, CSC, CSD, CSM)

[Time: 3 Hours] **[Max. Marks: 60]**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 10 marks. Answer all questions in Part A.
Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 10 marks and may have a, b, c as sub questions.

PART-A **(10 Marks)**

1. a)	What are the various functional units in the computer?	[1M]
b)	What are various phases in instruction cycle?	[1M]
c)	What is micro-programmed control unit?	[1M]
d)	List out data transfer instructions.	[1M]
e)	How subtraction operation is performed using addition?	[1M]
f)	What are the attractive features of Booth's algorithm?	[1M]
g)	List out the different types of ROM's.	[1M]
h)	What is Direct Memory access?	[1M]
i)	What is pipelining?	[1M]
j)	List out interconnection structures.	[1M]

PART-B **(50 Marks)**

2.a)	List out the Computer Instructions and Explain about it.	[5M]
b)	Explain in detail about Arithmetic micro-operations.	[5M]
	OR	
3.a)	Show that the block diagram of the hardware that implements the following register transfer statement P: R2←R1.	[6M]
b)	Narrate the three- state bus buffers with neat sketch.	[4M]
4.	Draw and explain the micro program sequencer for a control memory.	[10M]
	OR	
5.	Explain the following instructions with examples.	
a)	Data manipulation.	[5M]
b)	Program control.	[5M]
6.	Explain about fixed point and floating point representation.	[10M]
	OR	
7.	Draw the Flowchart and write algorithm for multiplication with an example.	[10M]
8.	How asynchronous data transfer operations can be performed? Explain it with the help of a diagram.	[10M]
	OR	
9.	What is Cache Memory? Explain in detail its mapping functions.	[10M]
10.	Explain briefly about arithmetic pipeline with neat diagram.	[10M]
	OR	
11.a)	What is inter processor communication mechanism? Explain how synchronization is provided in IPC?	[6M]
b)	Elaborate the cache coherency.	[4M]

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