Code No.: CS302PC | R20 | H.T.No. | | | 8 | R | | | | | |

CMR ENGINEERING COLLEGE: : HYDERABAD
UGC AUTONOMOUS
II–B.TECH–I–Semester End Examinations (Supply) - December- 2024
COMPUTER ORGANIZATION AND ARCHITECTURE
(Common to CSE, IT, CSC & CSM)

[Time: 3 Hours] **[Max. Marks: 70]**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 20 marks. Answer all questions in Part A.
Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 10 marks and may have a, b, c as sub questions.

PART-A **(20 Marks)**

1. a) Draw the the basic functional units of computer? [2M]
   b) What is bus? What are the different buses in a cpu? [2M]
   c) What is branch field? [2M]
   d) What is reverse polish notation? Give an example. [2M]
   e) Obtain the 9's complement of 12349876. [2M]
   f) Explain the floating point representation with examples. [2M]
   g) List the difference between static RAM and dynamic RAM. [2M]
   h) Define Virtual memory. [2M]
   i) What is parallel processing? [2M]
   j) What do you mean by vector interrupt? Explain. [2M]

PART-B **(50 Marks)**

2. Describe the Arithmetic Logic shift unit with neat diagram and examples. [10M]

OR

3.a) Draw the block diagram for the hardware that implements the following statements x+yz: AR← AR+BR where AR and BR are teo n-bit registers and x,y and z are control variables. Include the logic gates for the control function. [5M]
   b) Using a 4-bit counter with parallel load and a 4-bit adder, draw a block diagram that shows how to implement the following statements: x: R1← R1+R1 Add R2 to R1 x'y : R1← R1+1 Increment R1 where R1 is a counter with parallel load and R2 is a 4-bit register. [5M]

4. What is an addressing mode? Explain any four types of addressing modes, with suitable examples. [10M]

OR

5.a) Describe the conditional branching with block diagram. [5M]
   b) Explain the computer hardware configuration with neat diagram. [5M]

6.a) Perform the arithmetic operations (+42) + (-13) and (-42)-(-13) in binary using signed-2's complement representation for negative numbers. [5M]
   b) Derive the circuits for a 3-bit parity generator and 4-bit parity checker using an even-parity bit. [5M]

OR

7.a) Draw the Flow chart of add and subtract operations. [6M]
   b) Write the algorithm for adding and subtracting numbers in signed-2's complement representation. [4M]

8. Discuss the Memory Hierarchy in computer system with regard to Speed, Size and Cost. [10M]

OR

9. Explain the following.
   a) Auxiliary Memory. [5M]
   b) Associative Memory. [5M]

10.a) Describe RISC and CISC characteristics. [5M]
   b) Demonstrate the solution for Cache Coherence. [5M]

OR

11. Discuss the implementation of Instruction pipeline with an example. [10M]

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