Code No.: R22CS58351PE | R22 | H.T.No. | | | 8 | R | | | | | |

CMR ENGINEERING COLLEGE: : HYDERABAD
UGC AUTONOMOUS
II–M.TECH–I–Semester End Examinations (Regular) - January- 2025
ADVANCED COMPUTER ARCHITECTURE (PE-V)
(CSE)

[Time: 3 Hours] **[Max. Marks: 60]**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 10 marks. Answer all questions in Part A.
Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 10 marks and may have a, b, c as sub questions.

PART-A **(10 Marks)**

1. a)	Define parallel computing and give an example.	[1M]
b)	What is program partitioning?	[1M]
c)	Define scalability in parallel systems.	[1M]
d)	What are the performance metrics used in scalable systems?	[1M]
e)	Define shared memory architecture.	[1M]
f)	Write one difference between linear and non-linear pipeline processors.	[1M]
g)	Define vector processing.	[1M]
h)	What is message-passing?	[1M]
i)	What are latency-hiding techniques?	[1M]
j)	Mention one difference between fine-grain and coarse-grain multicomputers.	[1M]

PART-B **(50 Marks)**

2.	Compare PRAM and SIMD models with examples.	[10M]
	OR	
3.	Illustrate the conditions of parallelism with real-world examples.	[10M]
4.	Analyze the performance trade-offs in virtual memory technology.	[10M]
	OR	
5.	Explain the principles of scalable performance with examples.	[10M]
6.	Illustrate the design and working of an instruction pipeline.	[10M]
	OR	
7.	Analyze the functioning of backplane bus systems in parallel architectures.	[10M]
8.	Compare the architectures of multiprocessors and multicomputers.	[10M]
	OR	
9.	Evaluate the efficiency of CM-5 connection machines.	[10M]
10.	Illustrate the working of a dataflow processor with a diagram.	[10M]
	OR	
11.	Analyze the challenges in designing hybrid architectures.	[10M]

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