Code No.: EC57101PC | R20 | H.T.No. | | | 8 | R | | | | | | |

CMR ENGINEERING COLLEGE: : HYDERABAD

UGC AUTONOMOUS

I–M.Tech–I–Semester End Examinations (Regular) July- 2021

DIGITAL DESIGN AND VERIFICATION

(VLSI System Design)

[Time: 3 Hours] **[Max. Marks: 70]**

*1. Answer Any **FIVE** Questions. Each Question Carries 14 Marks*
2. Illustrate your answers with NEAT sketches wherever necessary.

5 x 14M=70M

1. a. Explain the architecture of booth multiplier.
   b. List different challenges in the clock distribution and Explain in detail.

2. a. Explain the blocking and non blocking statements with examples.
   b. Write the short notes on following.
   i. verilog data types
   ii. What is Verilog AMS? How is it different from HDL or Verilog?

3. a. List different modeling styles in verilog and VHDL. Explain them with an example for a sequential circuit.
   b. What is antenna effect? Explain methods to remove them.

4. a. list different functional verification approaches. Explain each with an example.
   b. Explain the role of scripting languages in verification.

5. a. Explain the terms Zero wire load model and custom wire load model in detail.
   b. Explain the need of IR Drop analysis in detail.

6. a. Explain current challenges in Physical design.
   b. List the steps of Physical Design flow. Explain each in detail.

7. a. Explain FPGA and ASCI Design flow.
   b. Draw and explain the architectures of PROM, PLA, PAL, and PLD.

8. a. Explains Randomization in System Verilog with an example.
   b. Explain different procedural statements in system verilog.

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