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Code No.: R22EC57101PC | R22 | H.T.No. | | | 8 | R | | | | | |

CMR ENGINEERING COLLEGE: : HYDERABAD
UGC AUTONOMOUS
I–M.TECH–I–Semester End Examinations (Regular) - March- 2024
DIGITAL DESIGN & VERIFICATION
(VLSISD)

[Time: 3 Hours] **[Max. Marks: 60]**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 10 marks. Answer all questions in Part A.
Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 10 marks and may have a, b, c as sub questions.

PART-A **(10 Marks)**

1. a) What is Sequential logic? [1M]
   b) List the types of flip-flops. [1M]
   c) Define Keyword in Verilog HDL. [1M]
   d) What is Verilog HDL used for? [1M]
   e) What does wire in Verilog HDL refer to? [1M]
   f) What is randomization? [1M]
   g) Write an example for wire load model. [1M]
   h) What is crosstalk? [1M]
   i) Define PLA. [1M]
   j) What is Programmable Interconnection? [1M]

PART-B **(50 Marks)**

2. Verify the universal property of NOR gate by realizing AND,OR,NAND,XOR and XNOR gates. [10M]

OR

3. Multiply (-6) and (2) using Booth's multiplier and write the process in details. [10M]

4. a. Compare Combinational and Sequential Logic. [5M]
   b. What are the features of Verilog HDL? [5M]

OR

5. a. Write a Verilog Program for 3 to 8 Decoder. [5M]
   b. Write a Verilog code for JK Flip-Flop. [5M]

6. What are the different Data types in Verilog HDL? [10M]

OR

7. What are differences between Initial and Always process statements in Verilog HDL? [10M]

8. What are different roots challenges? [10M]

OR

9. Write short notes on time delays with switch primitives relevant to switch level modelling. [10M]

10. Implement the following Boolean expression with the help of Programmable Array Logic (PAL) [10M]
X =AB + AC'
Y= AB' + BC'

OR

11. What is the difference between FPGA and ASIC design? [10M]

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