Code No.: DS405PC | R20 | H.T.No. | | | 8 | R | | | | | |

CMR ENGINEERING COLLEGE: : HYDERABAD
UGC AUTONOMOUS
II–B.TECH–II–Semester End Examinations (Supply) - July- 2024
COMPUTER ORGANIZATION AND ARCHITECTURE
(CSD)

[Time: 3 Hours] **[Max. Marks: 70]**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 20 marks. Answer all questions in Part A.
Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 10 marks and may have a, b, c as sub questions.

PART-A **(20 Marks)**

1. a) Difference between Computer Organization and Computer Architecture. [2M]
   b) Explain binary adder. [2M]
   c) Define pipeline register. [2M]
   d) Explain relative address mode. [2M]
   e) Convert the decimal number 1231 to binary. [2M]
   f) Explain BCD subtraction. [2M]
   g) Define vectored and interrupt. [2M]
   h) What is auxiliary memory? [2M]
   i) Define MIMD. [2M]
   j) Sketch how a 2* 2 interchange switch operates. [2M]

PART-B **(50 Marks)**

2. Explain how instruction is decoded along with timing and control diagram. [10M]

OR

3. Explain how all the arithmetic, logic and shift operations can be performed using single unit. [10M]

4. Illustrate the structure of a micro program sequencer. [10M]

OR

5. Convert the following arithmetic expressions from infix to revers polish notation. [10M]
   i) A * B + C * D + E * F
   ii) A + B * [C * D + E * (F + G)]

OR

6. Summarize the decimal fixed point representation. Perform the arithmetic operation (+42) + (-13) in binary using 2's complement. [10M]

OR

7. Illustrate Booth multiplication algorithm. Multiply 010111 with 110110 using Booth's Algorithm. [10M]

8. Explain data transfer using handshaking protocol. [10M]

OR

9. Elaborate the hardware organization of an associate memory. [10M]

10. Explain Delayed load and Delayed branch [10M]

OR

11. Difference between the CISC and RISC characteristics. [10M]

****