Code No.: CS302PC

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CMR ENGINEERING COLLEGE: : HYDERABAD UGC AUTONOMOUS

II-B.TECH-I-Semester End Examinations (Supply) - February- 2024 COMPUTER ORGANIZATION AND ARCHITECTURE (Common to CSE, IT, CSC & CSM)

ron.	(Common to CSE, 11, CSC & CSIVI)	
[Time: 3 Hours]		[arks: 70]
Note:	This question paper contains two parts A and B.	-
	Part A is compulsory which carries 20 marks. Answer all questions in Part A.	
Part B consists of 5 Units Anguar any one full question from soil with Early and		
Part B consists of 5 Units. Answer any one full question from each unit. Each question		
	carries 10 marks and may have a, b, c as sub questions.	
	PART-A	(20 Marks)
1 0)		
1. a)	Differentiate logical shift and arithmetic shift	[2M]
b)	Define register transfer language?	[2M]
c)	Differentiate micro operation and micro instruction	[2M]
d)	What is control word and how many fields it consists	[2M]
e)	What is restoring method in division algorithm?	[2M]
f)	Obtain the 10's complement of 123900 decimal number	[2M]
g)	What is memory hierarchy?	
h)	Define Associative memory.	[2M]
i)	Differentiate between RISC and CISC	[2M]
		[2M]
j)	Define cache coherence	[2M]
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2	PART-B	(50 Marks)
2.	What is bus? What are different types of buses used in computers? Discuss their uses	[10M]
	OR	
3.	Explain the Arithmetic and Logic micro operations with hardware implementation	[10M]
		[]
4. a)	Explain about stack organization used in processors. What do you understand by regist	ter [5M]
	stack?	[5141]
b)	What is an effective address? Explain instruction format.	[5M]
-)	OR	
5.	What are addressing modes? List and explain different addressing modes with suitable	1. [10]
٥.		ole [10M]
	examples.	
6 0)	Describe the desired and a Control of the control of the	***
6. a)	Describe the derivation procedure of addition and subtraction algorithms.	[5M]
b)	Show the systematic multiplication process of $(-15) \times (-16)$ using Booth's Algorithm.	[5M]
	OR	
7. a)	Draw the flow chart for multiplication algorithms.	[5M]
b)	Drive an algorithm for evaluating the square root of a binary fixed-point number.	[5M]
	g	[5141]
8.	With a neat schematic diagram, explain about DMA controller and its mode of da	ta [10M]
	transfer.	na [TOWI]
	OR	
9.	Explain the following.	[10] 43
		[10M]
a)	Cache Memory.	
b)	Virtual Memory.	
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10.	What is pipelining? How it improves the performance of computing? Explain.	[10M]
	OR	
11.	Discuss the implementation of arithmetic pipeline.	[10M]
