Code No.: AD504PC

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CMR ENGINEERING COLLEGE: : HYDERABAD UGC AUTONOMOUS

III-B.TECH-I-Semester End Examinations (Regular) - January- 2024 AUTOMATA AND COMPILER DESIGN (AI&DS)

[Time: 3 Hours] [Max. Marks: 70]

Note: This question paper contains two parts A and B.

Part A is compulsory which carries 20 marks. Answer all questions in Part A.

Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 10 marks.

	PART-A	(20 Marks)
1. a) b) c) d) e) f) g) h) i)	Define what is alphabet. Write the formal definition of Deterministic Finite Automata. List out different phases of Compiler. What is the purpose of lexical analyzer in compiler design? Define Context Free Grammar. What are the advantages of Top Down Parser? Write a short note on Flow graph. What is Dynamic storage allocation? What is common sub-expression? Give an Example. What are the uses of DAG?	[2M] [2M] [2M] [2M] [2M] [2M] [2M] [2M]
2.	PART-B Explain the procedure of converting Moore to Mealy machine with an example.	(50 Marks) [10M]
3.	OR Illustrate the conversion procedure of NFA to DFA.	[10M]
4.	Explain equivalence of NFA and regular expression with example. OR	[10M]
5.	Write about input buffering and recognition of tokens.	[10M]
6.	Write the comparison among SLR Parser, LALR parser and Canonical LR Parser. OR	[10M]
7.	Write the short note on: i. Abstract syntax tree. ii. Polish notation. iii. Three address code.	[10M]
8.	Describe briefly about storage allocation strategies.	[10M]
9.	OR What is code optimization? Explain in detail about peep-hole Optimization.	[10M]
10.	What are the properties of code generation phase and also discuss the Design Issue this phase.	es of [10M]
11.	OR Describe about register allocation and assignment.	[10M]
11.	Describe about register anocation and assignment.	[IOIVI]