Code No.: EC603PC | R20 | H.T.No. | | | 8 | R | | | | | |

CMR ENGINEERING COLLEGE: : HYDERABAD
UGC AUTONOMOUS
III–B.TECH–II–Semester End Examinations (Regular) - May- 2023
VLSI DESIGN
(ECE)

[Time: 3 Hours] **[Max. Marks: 70]**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 20 marks. Answer all questions in Part A.
Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 10 marks and may have a, b, c as sub questions.

PART-A **(20 Marks)**

1. a) What is Body Effect? [2M]
   b) Define Figure of Merit. [2M]
   c) List the various Color Coding used in Stick Diagram. [2M]
   d) Define Scaling. [2M]
   e) What is Switch Logic? [2M]
   f) Define Fan out. [2M]
   g) Draw the circuit diagram of SRAM cell. [2M]
   h) What is Parity Generator? [2M]
   i) Write the abbreviation of FPGA. [2M]
   j) What are Functionality Tests? [2M]

PART-B **(50 Marks)**

2. Draw the Fabrication steps of NMOS Transistor and explain its operation in detail. [10M]

OR

3. Illustrate the relationship between I_{ds} versus V_{ds} of MOSFET. [10M]

4. Draw the Flow Chart of VLSI Design Flow and explain the operation of each step-in detail. [10M]

OR

5. Explain about Lambda Based design rules for Wires and Transistors. [10M]

6. Explain the effect of Cascaded Inverters in driving large capacitive loads. [10M]

OR

7. Describe Wiring Capacitance. [10M]

8.a) Explain about Serial Access Memories. [5M]
   b) Compare SRAM and DRAM. [5M]

OR

9.a) Draw the logic diagram of Zero/One Detector and explain its operation. [5M]
   b) Explain about different types of ROM. [5M]

10.a) Compare various Programmable Devices. [6M]
   b) What are the factors that are influencing low power design? [4M]

OR

11. Explain the architecture of FPGA with neat diagram. [10M]

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