Code No.: R22EC57202PC/EC57202PC | R22/R20 | H.T.No. | | | 8 | R | | | | | |

CMR ENGINEERING COLLEGE: : HYDERABAD
UGC AUTONOMOUS
I–M.TECH–II–Semester End Examinations (Regular & Supply) – September- 2023
LOW POWER VLSI DESIGN
(VLSI SD)

[Time: 3 Hours] **[Max. Marks: 60]**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 10 marks. Answer all questions in Part A.
Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 10 marks and may have a, b, c as sub questions.

PART-A **(20 Marks)**

1. a)	Define Dynamic power.	[1M]
b)	What is mean by scaling?	[1M]
c)	What is the effect of Glitch?	[1M]
d)	Define clock skew.	[1M]
e)	What is mean by Retiming?	[1M]
f)	What is the main limitation of Ripple carry adder?	[1M]
g)	List out the advantages and disadvantages of SRAM.	[1M]
h)	Why refreshing operation is required in DRAM?	[1M]
i)	What is the major disadvantage of variable length instruction set?	[1M]
j)	Compare register variables with memory variables.	[1M]

PART-B **(50 Marks)**

2.	Discuss in detail different sources of power dissipation in digital ICs.	[10M]
	OR	
3.a)	What are the four recurring themes in low power? Elaborate	[5M]
b)	Briefly discuss the mechanism of power consumption in CMOS circuits.	[5M]
4.	Design the following dynamic flip-flops:	
a)	C^2MOS	[4M]
b)	Precharged TSPC	[3M]
c)	Non-precharged TSPC	[3M]
	OR	
5.	Demonstrate the types of high-performance energy recovery CMOS Approaches.	[10M]
6.	Discuss in detail the simulation based and probabilistic based power estimation techniques.	[10M]
	OR	
7.	Design the following types of Multipliers:	
a)	8-bit Array Multiplier	[5M]
b)	8-bit Wallace tree multiplier	[5M]
8.	Discuss in detail about low power SRAM circuits.	[10M]
	OR	
9.	Discuss DRAM circuits by emphasizing charging capacitance for the memory array.	[10M]

10. Briefly discuss several possible low-power implementation options and their suitability for microprocessor design. [10M]

OR

11. Discuss briefly the following architectural issues that may be addressed w.r.t low power Microprocessor designs:
    a) Datapath design [5M]
    b) Cache effects [5M]

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