Code No.: EC57202PC | R20 | H.T.No. | | | 8 | R | | | | | |

CMR ENGINEERING COLLEGE: : HYDERABAD
UGC AUTONOMOUS
I–M.TECH–II–Semester End Examinations (Supply) - March- 2023
LOW POWER SYSTEM DESIGN
(VLSISD)

[Time: 3 Hours] **[Max. Marks: 60]**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 20 marks. Answer all questions in Part A.
Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 10 marks and may have a, b, c as sub questions.

PART-A **(20 Marks)**

1. a) What is mean by technology scaling? [2M]
   b) What is mean by dynamic power dissipation? [2M]
   c) Design pseudo-N-MOS inverter. [2M]
   d) What is a single driver scheme? What is the advantage of it? [2M]
   e) List out the advantages of the array multiplier. [2M]
   f) List out different types of adder architectures. [2M]
   g) List out different sources of power dissipation in memory subsystem. [2M]
   h) Compare SRAM and DRAM. [2M]
   i) Define Register Variables and Memory Variables. [2M]
   j) What are the two standard choices for write policy? What is the difference between them? [2M]

PART-B **(50 Marks)**

2.a) Are there any constraints on reducing Vt? Elaborate. [4 M]
   b) Explain the impact of V_{DD}, L and Tox scaling on MOSFET current and inverter speed. [6 M]

OR

3. Briefly discuss the mechanism for power consumption in CMOS circuits. [10M]

4. Discuss the effect of different switching probabilities at different nodes in a circuit. [10M]

OR

5.a) Design the block diagram of a 4-stage, shift-register cell built from T-gates and explain the same? [5M]
   b) Discuss the reversible pipeline using the shift register approach. [5M]

6. Explain the following power minimizing techniques:
   a) Technology decomposition for low power [5M]
   b) Precomputation Logic [5M]

OR

7. Design an 8-bit Array Multiplier and explain. [10M]

8. Discuss in detail data retention sources of power dissipation in DRAM and SRAM. [10M]

OR

9. Discuss the following low power DRAM circuits:
   a) Active Power Reduction [5M]
   b) Data Retention Power Reduction [5M]

10. Discuss the following w.r.t choosing the supply voltage: [10M]
    i. Why Voltage Is So Important
    ii. Moving From 5 V to 3.3 V
    iii. Moving Below 3.3 V

OR

11. Briefly discuss the following possible implementation options for low power and their suitability for microprocessor design:
    a) Logic Synthesis [3M]
    b) Parallelism [3M]
    c) Minimizing Switching [4M]

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