Code No.: EC57202PC | R20 | H.T.No. | | | 8 | R | | | | | |

CMR ENGINEERING COLLEGE: : HYDERABAD
UGC AUTONOMOUS
I–M.TECH–II–Semester End Examinations (Supply) - Feb- 2022
LOW POWER SYSTEM DESIGN
(VLSI SD)

[Time: 3 Hours] **[Max. Marks: 70]**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 20 marks. Answer all questions in Part A.
Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 10 marks and may have a, b, c as sub questions.

PART-A **(20 Marks)**

1. a) Explain the need for low power circuit design? [2M]
   b) What are the limitations of low power designing? [2M]
   c) Write about Pipelining method for low power circuit design? [2M]
   d) Write a short note on low power dissipation measures? [2M]
   e) Write about the classification of multipliers? [2M]
   f) What is the effect of feature scaling on power dissipation? [2M]
   g) Write a note on MASK level measures for low power circuit design? [2M]
   h) What are the different low power techniques for SRAM? [2M]
   i) List various low power design techniques for microprocessors? [2M]
   j) What is resonant clocking? [2M]

PART-B **(50 Marks)**

2. What are the various limitations of low voltage low Power design? Explain? [10M]

OR

3. With neat sketches, Explain variable threshold CMOS inverter circuit? [10M]

4. a) Describe static and semi-static flip flops with neat diagrams? [5M]
   b) Define clock skew? How clock skew is calculated in timing analysis? [5M]

OR

5. Explain the need for Low-power latches and flip flops? [10M]

6. With the neat diagrams explain about Booth multiplier? [10M]

OR

7. Explain the different configurations of full adder circuit? [10M]

8. a) Show the differences between DRAM and SRAM? [4M]
   b) Discuss low power SRAM circuits with neat diagrams. [6M]

OR

9. Analyze the various techniques at architectural level used to design low power memories? [10M]

10. Explain implementation problems of low power design systems? [10M]

OR

11. Explain the architectural tradeoffs that need to be considered for choosing power and supply voltage? [10M]

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