Code No.: DS305ES | R20 | H.T.No. | | | 8 | R | | | | | |

# CMR ENGINEERING COLLEGE: : HYDERABAD
## UGC AUTONOMOUS
## II–B.TECH–I–Semester End Examinations (Supply ) – August - 2023
## DIGITAL LOGIC DESIGN
## (CSD)

**[Time: 3 Hours]** **[Max. Marks: 70]**

**Note:** This question paper contains two parts A and B.
Part A is compulsory which carries 20 marks. Answer all questions in Part A.
Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 10 marks and may have a, b, c as sub questions.

**PART-A** **(20 Marks)**

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|---|---|---|
| 1. a) | Using 10's complement subtract 72532 – 3250. | [2M] |
| b) | State and prove De Morgan theorems. | [2M] |
| c) | What are minterms and maxterms? Give examples for each. | [2M] |
| d) | Implement OR gate using NAND gates only. | [2M] |
| e) | What is a multiplexer? What is the function of a multiplexer's select input. | [2M] |
| f) | Write short notes on priority encoder. | [2M] |
| g) | What is the difference between latch and flip flop? | [2M] |
| h) | Write about race around condition. | [2M] |
| i) | What are PLAs and PALs? | [2M] |
| j) | Explain the role of Cache Memory in sequential circuits. | [2M] |

**PART-B** **(50 Marks)**

2. What is a Hamming code and encode data bits 0101 into a 7-bit even parity Hamming code. [10M]

**OR**

3. Give the comparison between 9's complement and 10's complement and perform the following subtraction by using 9's complement method. i) 18 – 06, ii) 39 – 23 [10M]

4. Simplify the following Boolean functions, using a four variable Karnaugh map method and implement the simplified function using NAND gates. [10M]
$F(A,B,C,D) = \Sigma(0,2,4,5,6,7,8,10,13,15)$

**OR**

5. Reduce the following function using K-Map Technique and implement using universal gate. [10M]
$f(P,Q,R,S) = \Sigma m(0,1,4,8,9,10) + d(2,11)$

6. What is a decoder? Construct a 4×16 decoder with two 3×8 decoders. [10M]

**OR**

7. Draw the logic circuit of a 3 to 8 decoder and explain its working. [10M]

8. Design and implement 3-bit ripple counter using J-K flip flop. Draw the state diagram, logic diagram and timing diagram for the same. [10M]

**OR**

9. Convert JK-Flip Flop in to T-Flip Flop. [10M]

10. Implement the following functions using PLA with three inputs and two outputs. [10M]
$F1(A, B, C) = \Sigma m(3, 5, 6, 7)$, $F2(A, B, C) = \Sigma m(0, 2, 4, 7)$.

**OR**

11. Design a memory decoder to select 1 number of 16KB EPROM IC and 1 number of 32KB RAM Ic. [10M]

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