Code No.: EC57101PC | R20 | H.T.No. | | | 8 | R | | | | | | |

CMR ENGINEERING COLLEGE: : HYDERABAD
UGC AUTONOMOUS
I–M.TECH–I–Semester End Examinations (Supply) – September - 2022
DIGITAL DESIGN AND VERIFICATION
(VLSI SD)

[Time: 3 Hours] **[Max. Marks: 70]**

Note: 1. Answer *any FIVE questions. Each question carries 14 marks.*
2. All questions carry equal marks.
3. Illustrate your answers with NEAT sketches wherever necessary.

5X14=70

1.	a)	Why do we use Clock Distribution in Digital Systems? Mention its issues.	[7M]
	b)	Design a 4-Bit Barrel Shifter.	[7M]
2.	a)	Demonstrate the various models of Verilog HDL Programming with examples.	[7M]
	b)	Implement a 3x8 Decoder and write the Verilog program for the same.	[7M]
3.	a)	Write a note on following System Verilog terms i. Data types ii. Routines	[7M]
	b)	Summarize the steps for designing test bench and its connection in System Verilog.	[7M]
4.	a)	Describe the current challenges in Physical Design.	[7M]
	b)	Outline the Process Effect of Antenna and Electromigration.	[7M]
5.	a)	Illustrate the Architecture of PAL and mention its applications.	[7M]
	b)	Draw the ASIC Design Flow and give in detail explanation.	[7M]
6.	a)	Multiply 2X3 using Booth's Multiplier Algorithm.	[7M]
	b)	Construct an ALU that performs both Arithmetic and Logical Operations.	[7M]
7.	a)	Differentiate between Verilog and VHDL Programming.	[7M]
	b)	How do you design a Verilog test bench? Explain with relevant example.	[7M]
8.	a)	Describe the Procedural Statements in System Verilog.	[7M]
	b)	Discuss the basics of Perl Scripting Language.	[7M]

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