Code No.: EC744PE | R20 | H.T.No. | | | 8 | R | | | | | |

CMR ENGINEERING COLLEGE: : HYDERABAD
UGC AUTONOMOUS
IV–B.TECH–I–Semester End Examinations (Regular) - November- 2023
DIGITAL CMOS IC DESIGN
(ECE)

[Time: 3 Hours] **[Max. Marks: 70]**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 20 marks. Answer all questions in Part A.
Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 10 marks and may have a, b, c as sub questions.

PART-A **(20 Marks)**

1. a) Draw the circuit diagram of a NMOS Inverter. [2M]
   b) Define Rise Time. [2M]
   c) Write the expressions for Sum and Carry in a Full-Adder circuit. [2M]
   d) Draw the representation of a CMOS Transmission Gate. [2M]
   e) Classify logic circuits based on their temporal behavior. [2M]
   f) Write the truth table of a Two input NAND gate. [2M]
   g) Write about Pass Transistors. [2M]
   h) What are the applications of a Shift Registers. [2M]
   i) Compare SRAM and DRAM. [2M]
   j) How many individual Memory Cells are available in a 32-Kbit ROM Array? [2M]

PART-B **(50 Marks)**

2. Draw the circuit diagram of a typical CMOS inverter. Explain its operation and derive the expression for threshold voltages. [10M]

OR

3. Draw the circuit diagram of a pseudo-NMOS inverter and explain its operation. [10M]

4. Draw the Two-input NMOS depletion-load NOR gate. Explain its operation in each with its truth table. [10M]

OR

5. Draw the Full CMOS implementation of $\overline{(AB+C)}$. Explain its operation in each with its truth table. [10M]

6. Illustrate the operation of a CMOS SR Latch circuit based on NOR gates along with its truth table. [10M]

OR

7. Discuss the implementation of CMOS D Latch along with its working principle and truth table. [10M]

8. Discuss about Voltage Bootstrapping in detail along with necessary expressions. [10M]

OR

9. Explain about the structure of Dynamic CMOS Transmission Gate. [10M]

10. Discuss the operation of a typical Three-Transistor DRAM cell along with its circuit diagram. [10M]

OR

11. Discuss the operation of SRAM cell along with its circuit diagram. [10M]

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