Code No.: CS302PC | R20 | H.T.No. | | | 8 | R | | | | | |

CMR ENGINEERING COLLEGE: : HYDERABAD
UGC AUTONOMOUS
II–B.TECH–I–Semester End Examinations (Supply) - August- 2023
COMPUTER ORGANIZATION AND ARCHITECTURE
(Common to CSE, IT, CSC & CSM)

[Time: 3 Hours] **[Max. Marks: 70]**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 20 marks. Answer all questions in Part A.
Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 10 marks and may have a, b, c as sub questions.

PART-A **(20 Marks)**

1. a)	Draw the Block diagram of a Digital Computer and Determine the importance of Digital Devices in modern era.	[2M]
b)	Discuss the Applications of Logic Micro Operations.	[2M]
c)	Define the i. Micro Operation ii. Micro Instruction iii. Micro Program iv. Micro Code.	[2M]
d)	Evaluate X= (A+B)*(C+D) and Describe the Zero address instruction.	[2M]
e)	Calculate the Binary and Octal value for $(2653)_{10}$.	[2M]
f)	Convert the following Decimal number to the base indicated i. 17562 to Octal ii. 11938 to Hexadecimal	[2M]
g)	Explain the IEEE Representation of Floating point numbers.	[2M]
h)	Find 2's complement of $(101011)_2$.	[2M]
i)	Define Mapping and List different types of Mapping Techniques.	[2M]
j)	List the three Cache Memory mapping techniques.	[2M]

PART-B **(50 Marks)**

2.a)	Describe Memory Reference Instruction.	[5M]
b)	Explain the Common Bus System.	[5M]
	OR	
3.a)	Discuss and Explain Instruction Cycle with a neat sketch.	[5M]
b)	Classify and Explain the Computer Instructions.	[5M]
4.a)	Construct circuit for Program Control Status bit condition.	[5M]
b)	Explain the functioning of a Micro Program Sequencer.	[5M]
	OR	
5.	Evaluate X= (A+B)*(C+D) using 3 address, 2 address, 1 address and 0 address instruction formats.	[10M]
6.	Explain Addition and Subtraction Algorithm with a flowchart.	[10M]
	OR	
7.	Evaluate the following: • 6-9 • 12+8 • 5-(-3) by using binary.	[10M]
8.a)	Distinguish Static and Dynamic RAM chips.	[[5M]
b)	Distinguish Programmed I/O and Interrupt Initiated I/O modes of Data Transfer.	[5M]
	OR	
9.	Describe IOP-CPU-IOP Communication with a neat diagram.	[10M]
10.	Explain Concept of Pipelining in detail.	[10M]
	OR	
11.a)	Differentiate RISC and CISC characteristics.	[5M]
b)	Explain Cache Coherence.	[5M]

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