Code No.: EC57201PC | R20 | H.T.No. | | | 8 | R | | | | | |

CMR ENGINEERING COLLEGE: : HYDERABAD
UGC AUTONOMOUS
I–M.TECH–II–Semester End Examinations (Supply) - Feb- 2022
ANALOG AND DIGITAL CMOS VLSI DESIGN
(VLSI SD)

[Time: 3 Hours] **[Max. Marks: 70]**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 20 marks. Answer all questions in Part A.
Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 10 marks and may have a, b, c as sub questions.

PART-A **(20 Marks)**

1.	a)	Explain the formal estimation of CMOS Inverter delay?	[2M]
	b)	Define stick diagram and layout diagram?	[2M]
	c)	State the disadvantages of dynamic CMOS logic?	[2M]
	d)	State the various types of power Dissipation?	[2M]
	e)	Explain bi-stability principle?	[2M]
	f)	What is meant by Pipelining?	[2M]
	g)	What is cascade amplifier?	[2M]
	h)	Explain why the Gilbert cell can operate as an analog voltage multiplier.	[2M]
	i)	What is the purpose of a current mirror?	[2M]
	j)	Why current mirror is used in differential amplifier?	[2M]

PART-B **(50 Marks)**

2. Draw the circuit diagram, stick diagram and layout for CMOS inverter [10M]

OR

3. a) Explain about the various layout design rules. [04M]
   b) Draw the static CMOS logic circuit for the following expressions [06M]
   i) Y=(ABCD)′
   ii) Y= [D(A+BC)]′

4. Discuss the transient analysis of CMOS Transmission gate by replacing it with resistor equivalent circuit. Design an EX-OR gate using Transmission gate Logic. [10M]

OR

5. a) What are various floor planning methods? Discuss in brief. [04M]
   b) Explain the delay in combinational logic network and how combinational delay can be reduced. [06M]

6. a) Draw the D latch by using CMOS logic and explain its operation in detail. [07M]
   b) Write short notes on SR latch in sequential MOS logic. [03M]

OR

7. a) What is race around condition? [04M]
   b) What is Giga Scale dilemma? [03M]
   c) What is high K metal gate technology? [03M]

8. Draw the small signal model of CS stage with source degeneration, also plot the drain current and transconductance of a CS device. [10M]

OR

9. Define and explain the following terms [05M]
   a) Common-Mode Input Range [05M]
   b) Common-Mode Rejection Ratio

10. What is Current Mirror .Explain the general properties of current mirrors with block diagram [10M]

OR

11. a) Draw and explain about a simple current mirror with Beta helper. [6M]
    b)Write a short notes on current sinks and sources [4M]

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