Code No.: CS403ES

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CMR ENGINEERING COLLEGE: : HYDERABAD UGC AUTONOMOUS

II-B.TECH-II-Semester End Examinations (Supply) - February- 2023 ANALOG & DIGITAL ELECTRONICS

(Common to CSE, CSC)

[Time: 3 Hours]

[Max. Marks: 70]

Note: This question paper contains two parts A and B.

Part A is compulsory which carries 20 marks. Answer all questions in Part A.

Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 10 marks and may have a, b, c as sub questions.

	PART-A	(20 Marks)
1. a) b) c) d) e) f) g) h) i)	Draw the Tunnel diode symbol. Draw PN Junction diode characteristics. Compare CE, CB, CC configurations. Draw self-bias circuit diagram. Draw MOSFET symbols. Explain the De Morgan's theorem. Minimize Boolean expression for AC+A'C+BC. Explain the EX-OR logic gate with truth table. Draw SR Flip flop logic diagram. Compare synchronous and asynchronous counters?	[2M] [2M] [2M] [2M] [2M] [2M] [2M] [2M]
2.	PART-B Explain the diode switching times and diode resistance and capacitance.	(50 Marks) [10M]
2.	OR	[]
3.	Explain the full rectifier with capacitor filter.	[10M]
4.a) b)	Explain the thermal runaway and stability. Explain the transistor at low frequencies of CE. OR	[5M] [5M]
5.a) b)	Explain the input transistor characteristics of CB configuration. Explain the CE amplifier with near circuit diagram.	[5M] [5M]
6.a) b)	Explain the TTL gates. Explain the FET CD amplifier.	[5M] [5M]
	OR	[6] 4]
7.a) b)	Compare logic families. Explain the low frequency JFET common source- amplifier.	[5M] [5M]
8.a) b)	Minimize Boolean expression using K Map. $F(A, B,C,D)=\sum m(0,1,4,5,8,9,13,15)$. Design Half subtractor.	[5M] [5M]
	OR	
9.a) b)	Convert into standard SOP from for F(a, b, c)=a'b+a+bc'. Draw the full adder logic diagram.	[5M] [5M]
10.a) b)	Design of 3 bit up counter using asynchronous (ripple) counter. Explain the SR Flip flop using NAND Latch.	[5M] [5M]
11.a) b)	Explain 4 bit SISO shift register. Explain the Random-access memory.	[5M] [5M]