Code No.: IT301ES | R20 | H.T.No. | | | 8 | R | | | | | | |

CMR ENGINEERING COLLEGE: : HYDERABAD
UGC AUTONOMOUS
II–B.TECH–I–Semester End Examinations (Regular) - February- 2023
ANALOG & DIGITAL ELECTRONICS
(Common to IT, CSM and AI&DS)

[Time: 3 Hours] **[Max. Marks: 70]**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 20 marks. Answer all questions in Part A.
Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 10 marks and may have a, b, c as sub questions.

PART-A **(20 Marks)**

1. a) What is the efficiency of Half wave rectifier and Full wave rectifier? [2M]
   b) Draw PN Junction diode. [2M]
   c) Compare CB, CE, CC Configuration? [2M]
   d) Mention important characteristics of CE amplifier. [2M]
   e) Write Demorgans Law? [2M]
   f) Draw CMOS Inverter? [2M]
   g) How do you obtain dual of an expression? [2M]
   h) What is don't-care conditions? [2M]
   i) Define the following terms of a flip flop. [2M]
      i) Hold time ii) Set up time
   j) Explain about the memory read operations? [2M]

PART-B **(50 Marks)**

2. Draw and explain the V-I characteristics of a tunnel diode? [10M]

OR

3. Derive the expression for ripple factor for the circuit FWR ? [10M]

4. Draw the circuit diagram of an NPN junction transistor in CE configuration and describe its characteristics. [10M]

OR

5. Explain the input and output characteristics of common base configuration. [10M]

6. Draw CMOS 2 INPUT NAND gate and then explain the same. [10M]

OR

7. Draw a totem-pole output buffer with a TTL gate. Explain its operation? [10M]

8. Design a 32:1 multiplexer using 16:1 Mux and 2:1 multiplexer? [10M]

OR

9. Simplify the following Boolean function using K-Map. [10M]
   $F(A, B, C, D) = \sum m (0, 2, 3, 6, 7, 8, 10, 12, 13)$

10. Draw the logic diagram of a four-bit binary-ripple countdown counter using flip-flops that trigger on the positive edge of the clock. [10M]

OR

11. Realize D and T flip flops using Jk flip flops. [10M]

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