Code No.: CS8202PC | R20 | H.T.No. | | | 8 | R | | | | | |

CMR ENGINEERING COLLEGE: : HYDERABAD
UGC AUTONOMOUS
I–M.TECH–II–Semester End Examinations (Regular) – September-2021
ADVANCED COMPUTER ARCHITECTURE
(CSE)

[Time: 3 Hours] **[Max. Marks: 70]**

1. *Answer Any **FIVE** Questions. Each Question Carries 14 Marks*
2. *All Questions Carry Equal Marks*
3. *Illustrate your answers with NEAT sketches wherever necessary.*

5X14=70

1.	a)	List the Challenges of Parallel Processing systems in detail	[7M]
	b)	Argue the similarities and differences between Multimedia SIMD computers and MIMD	[7M]
2.	a)	Explain Amdahl's law and elaborate how the speedup is quickly calculated using Amdahl's law.	[7M]
	b)	Take a suitable example to show that Super scalar processors allows a faster CPU throughput due to instruction level parallelism.	[7M]
3.	a)	Explain about 3 C's of Cache Miss.	[7M]
	b)	Express in detail about the optimizations of cache performance	[7M]
4.	a)	Design, Discuss and Contrast the following two approaches for building a parallel system. In this first approach, a small number of powerful processors is used in which each processor is capable of performing serial computations at a given rate, Ψ. In the second approach, a large number of simple processors are used in which each processor is capable of performing serial computations at a lower rate, $\Phi < \Psi$. What is the condition under which the second system will execute a given computation more slowly than a single processor of the first system?	[7M]
	b)	Compare and Contrast the various cache coherence mechanisms	[7M]
5.	a)	Enumerate the various latency hiding techniques. Explain them, and evaluate their applicability	[7M]
	b)	List, analyze and compare the various classifications of parallel structures. Where do you think each of them could be used?	[7M]
6.	a)	Describe the conditions of Parallelism	[7M]
	b)	Discuss and evaluate the various program flow mechanisms and list out their usability	[7M]
7.	a)	Discuss and describe a typical superscalar architecture for a RISC processor	[7M]
	b)	Analyze the ways for improving Memory Performance Inside a DRAM Chip.	[7M]

8. a) Calculate how many clock cycles will take execution of this segment on the simple pipeline without forwarding or bypassing when result of the branch instruction (new PC content) is available after WB stage. Show timing of one loop cycle in figure below: [7M]

Instruction	Clock cycle number 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17
LW R1, 0 (R4)	
LW R2, 400 (R4)	
ADDI R3,R1,R2	
SW R3, 0 (R4)	
SUB R4, R4, #4	
BNEZ R4, L1	

b) The 5 stages of the processor have the following latencies: [7M]

S.no	Fetch	Decode	Execute	Memory	Writeback
a.	300ps	400ps	350ps	550ps	100ps
b.	200ps	150ps	100ps	190ps	140ps

Assume that when pipelining, each pipeline stage costs 20ps extra for the registers between pipeline stages.

(a) Non-pipelined processor: what is the cycle time? What is the latency of an instruction? What is the throughput?

(b) Pipelined processor: What is the cycle time? What is the latency of an instruction? What is the throughput?

If you could split one of the pipeline stages into 2 equal halves, which one would you choose? What is the new cycle time? What is the new latency? What is the new throughput?

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