Code No.: EC57203PE | R20 | H.T.No. | | | 8 | R | | | | | |

CMR ENGINEERING COLLEGE: : HYDERABAD
UGC AUTONOMOUS
I–M.TECH–II–Semester End Examinations (Supply) - Feb- 2022
SOC DESIGN
(VLSI SD)

[Time: 3 Hours] **[Max. Marks: 70]**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 20 marks. Answer all questions in Part A.
Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 10 marks and may have a, b, c as sub questions.

PART-A **(20 Marks)**

1.	a)	What are the ASIC types?	[2M]
	b)	What is the ASIP and explain in brief?	[2M]
	c)	Draw the NISC Architecture?	[2M]
	d)	What is the compilation and Synthesis?	[2M]
	e)	Discuss the clock tree design issues?	[2M]
	f)	Write short notes on Reconfigurable System with an example?	[2M]
	g)	Distinguish between Power gating and Clock gating	[2M]
	h)	Classify the power down techniques?	[2M]
	i)	What is the graph theory in Synthesizable constructs?	[2M]
	j)	What is the functioning fault tolerant design	[2M]

PART-B **(50 Marks)**

2.	Draw the SoC Design flow and explain the SoC design methodologies.	[10M]
	OR	
3.	Compare CISC, RISC and NISC approaches for SOC architectural issues?	[10M]
4.	Explain NISC Control Words methodology with NISC Applications and Advantages	[10M]
	OR	
5.	Explain the Architecture Description Languages (ADL) for design with neat sketch	[10M]
6.	Discuss about different Simulation models with examples	[10M]
	OR	
7.	Construct the Data path design and Control Logic?	[10M]
8.	Demonstrate the adaptive voltage scaling and its advantages?	[10M]
	OR	
9.	Illustrate about DCFS with examples?	[10M]
10.	Determine the different HDL coding techniques with examples.	[10M]
	OR	
11.	Analyze the synthesis report with single core and multi core systems	[10M]

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