Code No.: EC302PC | R20 | H.T.No. | | | 8 | R | | | | | |

CMR ENGINEERING COLLEGE: : HYDERABAD
UGC AUTONOMOUS
II–B.TECH–I–Semester End Examinations (Supply)- June- 2022
DIGITAL SYSTEM DESIGN
(ECE)

[Time: 3 Hours] **[Max. Marks: 70]**

Note: 1. Answer *any FIVE questions. Each question carries 14 marks.*
2. All questions carry equal marks.
3. Illustrate your answers with NEAT sketches wherever necessary.

5X14=70

1.	a)	i. Convert $(657)_8$ into Decimal. ii. Convert $(2348)_{10}$ into Hexadecimal.	[7M]
	b)	Implement the given boolean expression using AND, OR, and NOT Gates F= x y + x′ y′ + y′ z.	[7M]
2.	a)	Minimize the following expression using K-Map f = Σ m (1,3,5,8,9,11,15) +d (2,13).	[7M]
	b)	Develop a 4:16 Decoder using 3:8 Decoders with its Structural Diagram.	[7M]
3.	a)	Draw and explain the Logic Diagram of Positive Edge Triggered J-K Flip-Flop using NOR Gates with its Truth Table.	[7M]
	b)	Explain the operation of 4-Bit Johnson Counter using D-Flip Flops with the help of bit pattern.	[7M]
4.	a)	Design a 3-Bit Up/Down Counter which counts up when the control signal M=1.	[7M]
	b)	Explain the differences between Asynchronous and Synchronous Counters.	[7M]
5.	a)	Draw and explain CMOS 2-Input NAND Gate.	[7M]
	b)	Compare CMOS, TTL and ECL with reference to Logic Levels, DC Noise Margin, and Propagation Delay and Fan-Out.	[7M]
6.	a)	Convert $(110001.1010010)_2$ into Hexadecimal. Convert $(423.25)_{10}$ into Hexadecimal.	[7M]
	b)	Classify the Weighted Codes and Non-Weighted Codes.	[7M]
7.	a)	Design Full Adder using Half Adder and OR Gate.	[7M]
	b)	Minimize F(c,b,a)= Σ m(0,1,6,7) using NOR Gate.	[7M]
8.	a)	Convert T Flip Flop to D Flip Flop.	[7M]
	b)	Explain Twisted Ring Counter in brief with neat sketch.	[7M]

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