Code No.: CS302PC

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## CMR ENGINEERING COLLEGE: HYDERABAD UGC AUTONOMOUS

## II-B.TECH-I-Semester End Examinations (Regular) - January- 2022 COMPUTER ORGANIZATION AND ARCHITECTURE (Common to CSE, IT, CSC & CSM)

[Time: 3 Hours]

[Max. Marks: 70]

Note: This question paper contains two parts A and B.

Part A is compulsory which carries 20 marks. Answer all questions in Part A. Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 10 marks and may have a, b, c as sub questions.

	$\underline{PART-A} \qquad (20 \text{ M})$	Aarks)
1. a)	What is Bus?	[2M]
b)	Determine need of Register? Write the name of different type of Registers.	[2M]
c)	Discuss the principle operation of Microprogrammed control unit.	[2M]
d)	Define Processor clock.	[2M]
e)	List the steps of Booth's Multiplication algorithm.	[2M]
f)	Describe the IEEE representation of Floating point numbers?	[2M]
g)	Justify the need of I/O Interface?	[2M]
h)	Define Locality of Reference.	[2M]
i)	Determine the use of Instruction Pipelining?	[2M]
j)	Explain Cache Coherence problem?	[2M]
		Marks)
2.	a) Sketch and explain the Design of Control Unit?	[5M]
	b) Design the flowchart for Interrupt cycle and explain it.  OR	[5M]
3.	Explain the Arithmetic circuit with a neat diagram and derive the operations?	[10M]
4.	Explain the following Addressing Modes with suitable example each? a) Direct b) Immediate c)Indexed –Addressing Modes.	e [10M]
	OR	
5.	What are the different types of CPU organizations? Explain each organization with an example in detail.	e [10M]
6.	Evaluate $(2563)_{10}$ - $(6532)_{10}$ by using 9's and 10's complement and Explain the flowchart for Division algorithm?	r [10M]
	OR	
7.	a) Design the flowchart for Multiplication algorithm?	[5M]
	b) Illustrate 04*02 with the help of Multiplication algorithm?	[5M]
8.	Explain the block diagram of DMA transfer with a neat diagram?  OR	[10M]
9.	Consider a cache consisting of 256 blocks of 8 words each, for a total of 2048 words, an	d [10M]
	assume that the main memory is addressable by a 16-bit address. The main memory has 641	
	words which are divided into 8192 blocks of 8 words each. Find the number of bits in Tag Block and Word Field of the main memory address for direct mapping scheme.	5,
	and the state of the main memory address for direct mapping seneme.	
10.	Discuss the different conflicts of Instruction Pipelining and explain them?	[10M]
11.	a) Justify and explain the need of Pipelining in detail?	[5]
11.	b) Discuss Inter-process arbitration?	[5M] [5M]
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