Code No: 137JD

R16

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
B. Tech IV Year I Semester Examinations, July - 2021
VLSI DESIGN
(Common to ECE, EIE)

Time: 3 Hours **Max. Marks: 75**

Answer any Five Questions
All Questions Carry Equal Marks

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1. Evaluate the DC transfer characteristics of CMOS inverter. [15]

2. Derive the drain current of MOS device in different operating regions. [15]

3. With necessary illustrations explain the layout design rules and draw the layout diagram for four input NAND gate. [15]

4. Explain in detail about the need of scaling, scaling principles and effect of scaling on MOSFET device parameters. [15]

5. Derive the expression for time delay of a MOS device with cascaded inverters as drivers. [15]

6. Examine the concept of carry look ahead adder and discuss its advantages and disadvantages. [15]

7. Define shifter and give a short note on
   a) Barrel shifter.
   b) Logarithmic shifter. [7+8]

8. Explain the various design strategies for test. [15]

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