Code No: 153AN

R18

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
B. Tech II Year I Semester Examinations, March - 2021
DIGITAL SYSTEM DESIGN
(Electronics and Communication Engineering)

Time: 3 Hours **Max. Marks: 75**

Answer any five questions
All questions carry equal marks

1.a) Convert the following to Decimal and then to octal.
i) $(125F)_{16}$
ii) $(10111111)_2$
iii) $(4234)_5$.

b) How do you convert a gray number to binary? Generate a 4-bit gray code directly using the mirror image property. [7+8]

2.a) Find all the prime implicants of the function using Quine McClusky method $f(a,b,c,d) = \Sigma(7,9,12,13,14,15) + d(4,11)$.

b) Design a circuit that converts 8421 BCD code to XS-3 code. [8+7]

3.a) With a neat circuit diagram and waveforms explain the operation of Master Slave JK flip flop.

b) Explain the conversion of SR flip flop into JK and D flip flop with an excitation table. [8+7]

4.a) What are the capabilities and limitations of finite state machines? Explain.

b) Draw the diagram of Mealy type FSM for serial adder. [8+7]

5.a) Describe the operation of TTL logic circuit working as NAND gate.

b) Realize 2-input OR gates using CMOS logic and then explain its operation with the help of functional table. [7+8]

6.a) Convert the following expression into SOP and POS:
i) (AB+C)(B+C´D)
ii) x´+(x+y´)(y+z´)

b) Implement the switching function using $F = \Sigma m(0,1,3,4,12,14,15)$ using an 8 input MUX. [8+7]

7.a) Design a 3-bit synchronous counter with T-flip flop and draw the diagram.

b) Discuss the differences between combinational and sequential circuit. [9+6]

8.a) Mention the characteristics of different logic families. Also compare the performance of TTL, CMOS and ECL logic.

b) Design a synchronous sequential circuit which goes through the following states: 1, 3, 5, 3, 6, 1, 3, 5. [8+7]

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