R17

Code No: 5477AP

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

M. Tech II Semester Examinations, July/August - 2021

CMOS MIXED SIGNAL CIRCUIT DESIGN

(Embedded Systems and VLSI Design)

Time: 3 Hours **Max. Marks: 75**

Answer any five questions

All questions carry equal marks

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1. Find the capacitance values needed for a first-order switched-capacitor circuit such that its 3-dB point is at 10 kHz when a clock frequency of 100 kHz is used. It is also desired that the filter have zero gain at 50 kHz and the dc gain be unity. Assume C_A = 10 pF. [15]

2. What is switch sharing? Explain a low-Q switched-capacitor biquad filter without switch sharing. [15]

3.a) Explain the lock acquisition problem in PLL and how to increase acquisition range.
b) Explain the response of PLL to jitters. [8+7]

4. Explain the following applications of PLL.
a) Frequency Multiplication
b) Skew reduction. [8+7]

5. What are the disadvantages of binary-weighted resistor converters and explain how these disadvantages are overcome in R-2R-based converters. [15]

6. What is hybrid D/A converter? Explain any two hybrid D/A converters. [15]

7. Discuss a 4-bit interpolating A/D converter with interpolating factor of 4. [15]

8. What are the advantages of multi-bit oversampling converters over 1-bit oversampling converters. Explain dynamic element matching 3-bit D/A converter. [15]

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