R19

Code No: 5677AH

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

M.Tech I Semester Examinations, July/August - 2021

CAD FOR DIGITAL SYSTEMS

(Embedded Systems and VLSI Design)

Time: 3 Hours Max. Marks: 75

Answer any Five questions

All questions carry equal marks

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1.a) Compare MOS and CMOS characteristics.

b) Draw and explain the operation of a CMOS static RAM cell. [7+8]

2.a) What is the effect of scaling on device parameters in full and constant voltage scaling?

b) Estimate the total power required by a maximally packed 19 mm × 23 mm chip in 0.75μm CMOS technology. Note: Allow 10% area for routing and assume 500 MHz clock frequency. [7+8]

3.a) Develop a heuristic algorithm for finding a maximum bipartite subgraph in circle graphs.

b) Explain the graph search algorithm with an example. [10+5]

4. Develop an efficient algorithm to find a k-density MIS in circle graphs. [15]

5.a) Compare the performance of the simulated Annealing algorithm for different values of a.

b) Differentiate system level partitioning and chip-level partitioning. [10+5]

6. Implement a placement algorithm for high performance circuits which takes into account path delays instead of net delays. [15]

7. Discuss static and dynamic partitioning with an example. [15]

8. Write the VHDL code for 4:2 encoder and 4:2 priority encoder. [15]

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